38th IEEE COMPOUND SEMICONDUCTOR IC (CSIC) SYMPOSIUM

Program

Presenting:

ALL CSICS and No Cattle!

Oct 23rd – Oct 26th, 2016
Doubletree by Hilton
Austin, Texas,
USA

CO- SPONSORED BY
The IEEE Electron Devices Society,
The IEEE Solid-State Circuits Society, and
The IEEE Microwave Theory and Techniques Society.

SYMPOSIUM

Sunday, October 23rd, 2016
Short Course Continental Breakfast
SHORT COURSE 1: Terahertz SiGe HBT technologies: Creating the winning design engine
PRIMER COURSE I: Introduction to Si RFIC Design
Short Course Lunch
REGISTRATION for Symposium
SHORT COURSE 2: GaN and SiC technologies for Power Electronics
PRIMER COURSE II: Fundamentals of A/D Converters
CSIC Symposium Opening Cocktails

Monday, October 24th, 2016
REGISTRATION
Continental Breakfast
SYMPOSIUM OPENING
SESSION A: Plenary Session
SESSION B: Reconfigurable RF Components and Systems
SESSION C: GaN HEMT Physical Characterization
SESSION D: Millimeter-wave Circuits using State-of-the-Art Transistors
SESSION E: Mixed-Signal Circuits and Interconnects for 100G+ Systems
Exhibition Opening Reception
Technology Exhibition

Tuesday, October 25th, 2016
REGISTRATION
Technology Exhibition
Continental Breakfast
SESSION F: Broadband THz Systems and Applications
SESSION G: GaN on Diamond
PANEL SESSION 1: III-V vs. Si-Photonic Integrated Circuits (PIC) - What will survive the future?
Exhibition Lunch
SESSION H: High-Speed Circuits for Optical and Electrical Links
SESSION I: High-Power Amplifier Technology
SESSION J: Late-Breaking News Papers I
SESSION K: Noise and Non-Linear Modeling
PANEL SESSION 2: THz Metrology and Testing

Wednesday, October 26th, 2016
REGISTRATION
Continental Breakfast
SESSION L: GaN HEMT Modeling
SESSION M: E- and W-band Technology and Circuits
SESSION N: High Power GaN
SESSION O: Components for Advanced Optical Front-End
PANEL SESSION 3: Reconfigurable RF Systems, Fact or Fiction?
SESSION P: Low Noise Amplifiers
SESSION Q: Next Generation Device Technologies
SESSION R: Late-Breaking News Papers II
SESSION S: Late-Breaking News Papers III

Close of Symposium

AT A GLANCE

Sunday, October 23rd, 2016

7:00 a.m. – 8:00 a.m.	Prefunction Area (Registration)
7:00 a.m. – 8:00 a.m.	**Dewitt (Breakfast)**
7:30 a.m. – 3:00 p.m.	Austin (Short Course 1)
8:00 a.m. – 12:00 p.m.	Robertson (Primer I)
12:00 p.m. – 1:00 p.m.	**Dewitt (Lunch)**
3:00 p.m. – 8:00 p.m.	Prefunction Area (Registration)
3:00 p.m. – 7:00 p.m.	Austin (Short Course 2)
3:00 p.m. – 5:30 p.m.	Robertson (Primer II)
7:00 p.m. – 8:00 p.m.	**Dovers (Cocktails)**

Monday, October 24th, 2016

7:00 a.m. – 5:00 p.m.	Prefunction Area (Registration)
7:00 a.m. – 8:30 a.m.	**Dovers (Breakfast)**
8:30 a.m. – 9:00 a.m.	Phoenix North (Symposium Opening)
9:00 a.m. – 12:00 p.m.	Phoenix North (Plenary)
1:30 p.m. – 3:00 p.m.	Phoenix North (Session B)
1:30 p.m. – 2:40 p.m.	Austin (Session C)
3:30 p.m. – 5:00 p.m.	Phoenix North (Session D)
3:30 p.m. – 4:50 p.m.	Austin (Session E)
4:30 p.m. – 7:30 p.m.	Phoenix South/Central (Exhibition)
6:00 p.m. – 7:30 p.m.	**Phoenix South/Central (Reception)**

Tuesday, October 25th, 2016

7:00 a.m. – 5:00 p.m.	Prefunction Area (Registration)
7:00 a.m. – 3:30 p.m.	**Phoenix South (Exhibition)**
7:00 a.m. – 8:30 a.m.	**Phoenix South (Breakfast)**
8:30 a.m. – 10:10 a.m.	Phoenix North (Session F)
8:30 a.m. – 9:50 a.m.	Austin (Session G)
10:30 a.m. – 12:00 p.m.	Phoenix North (Panel 1)
12:00 p.m. – 1:30 p.m.	**Phoenix South (Exhibition Lunch)**
1:30 p.m. – 3:00 p.m.	Austin (Session H)
1:30 p.m. – 3:30 p.m.	Phoenix North (Session I)
3:30 p.m. – 5:00 p.m.	Phoenix North (Session J)
3:30 p.m. – 4:50 p.m.	Austin (Session K)
5:30 p.m. – 7:00 p.m.	Phoenix North (Panel 2)

Wednesday, October 26th, 2016

7:00 a.m. – 12:00 p.m.	Prefunction Area (Registration)
7:00 a.m. – 8:30 a.m.	**Phoenix South (Breakfast)**
8:30 a.m. – 9:50 a.m.	Phoenix North (Session L)
8:30 a.m. – 10:00 a.m.	Austin (Session M)
10:30 a.m. – 12:00 p.m.	Phoenix North (Session N)
10:30 a.m. – 12:00 p.m.	Austin (Session O)
12:00 p.m. – 1:30 p.m.	**Phoenix North (Panel 3)**
1:30 p.m. – 3:00 p.m.	Phoenix North (Session P)
1:30 p.m. – 3:10 p.m.	Austin (Session Q)
3:30 p.m. – 5:00 p.m.	Phoenix North (Session R)
3:30 p.m. – 5:00 p.m.	Austin (Session S)

5:00 p.m. End of Symposium

Visit us at: http://www.csics.org

CHAIR'S MESSAGE

It is with great pleasure that I invite you to be a part of the 2016 IEEE Compound Semiconductor IC Symposium (CSICS). Thanks to the efforts of the many dedicated volunteers on the organizing committee and the generous support of the IEEE Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits Societies, CSICS is proud to offer a world class technical program. For this 38th edition, CSICS will be held on October 23-26 in Austin, Texas.

From its origins in 1978 as an international gathering for distinguished experts to present their latest results in GaAs IC technology and Monolithic Microwave Integrated Circuit design, the symposium has become much more and now embraces GaN, InP, SiGe, nanoscale CMOS, and many other emerging technologies. This convergence allows CSICS to offer a perfect blend of state of the art IC performance, innovative design techniques, and advanced device technologies. There are no other events in the world where you can see GaN HPAs, InP THz PAs, 100 Gb/s CMOS/SiGe transceivers, GaN HEMT power devices, and advances in compact modeling all presented alongside each other.

Following its tradition, CSICS will include presentations from worldwide submissions on all aspects of the technology, from materials and device fabrication and modeling to IC design and testing, high-volume manufacturing, and system applications. It will also feature the very latest results in RF/microwave, millimeter-wave, THz, analog mixed signal, and optoelectronic integrated circuits.

On Sunday prior to the symposium opening, CSICS will offer topical short and primer courses. Taught by leading experts, the short courses are intended for both technologists and IC designers who seek a comprehensive understanding of the latest industry trends and techniques. The primer courses are intended to be tutorials, introducing the key concepts, techniques and practices for Si mixed signal and RF circuit design. This year we are pleased to offer two full primer courses for the first time: one on RF CMOS design and the other on DACs and ADCs.

As a complement to the technical program, the symposium includes numerous social events that allow participants to interact and network in a relaxed setting. These include the Sunday Evening Opening Reception, the Monday Evening Exhibition Opening Reception, and the Technology Exhibition Luncheon on Tuesday. On Tuesday evening, a bus service will be provided to see the nightlife and music on Austin's famous 6th Street. CSICS also offers a daily breakfast and AM/PM coffee breaks on Monday through to Wednesday.

Please join us at the Compound Semiconductor IC Symposium in Austin, Texas.

Harris (Chip) Moyer, Chair

2016 IEEE CSICS

CORPORATE BENEFACTORS

This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support for the Symposium by making contributions towards the cost of some of our social events.

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. To discuss any of the benefactor opportunities in more depth, please contact:

Harris (Chip) Moyer
Tel: +1 (310) 317-5784
E-mail: hpmoyer@hrl.com

As of this version, the Corporate Benefactors for the 2016 Compound Semiconductor IC Symposium are as follows.

Gold Level Benefactor

Qorvo

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all around you

Silver Level Benefactors

Keysight Technologies

KEYSIGHT TECHNOLOGIES

National Instruments

NATIONAL INSTRUMENTS

OMMIC

OMMIC
Innovating with III-V's

The Symposium Web Site www.csics.org has become a critical tool for the dissemination of information to prospective attendees, committee members and sponsors of the Symposium. Every year, the web site must be updated and maintained to effectively serve this purpose. We would like to acknowledge the following benefactor for providing the Symposium web site support for the 2016 CSIC Symposium:

II-VI

Media Partners and Other Partner Conferences

COMPOUND SEMICONDUCTOR
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Microwave Journal
Frequency Matters.

Power Amplifier Symposium

IEEE ITHERM CONFERENCE

INTERNATIONAL SYMPOSIUM FOR TESTING AND FAILURE ANALYSIS

Comments regarding the web site or any publicity materials should be directed to the Publicity Chair, The' Linh Nguyen (thelinh.nguyen@finisar.com). Links to our corporate benefactors appear on our symposium website.

GENERAL INFORMATION

IEEE 38th CSIC Symposium
Oct 23rd - Oct 26th, 2016
Doubletree by Hilton Hotel
Austin, Texas, USA

REGISTRATION

	Advance (Received by Sept. 23rd)	Regular (After Sept. 23rd or on site)
Symposium Registration		
IEEE Member	$700	$750
Non-IEEE	$750	$850
IEEE Life-Member	$350	$350
Student	$380	$440
One Day - IEEE Member[1]	$350	$430
One Day - IEEE Life Member[1]	$240	$240
One Day - Non-IEEE[1]	$390	$450
One Day - Student[1]	$240	$270
Short/Primer Course		
Short Course 1+2	$500	$500
Short Course 1+2 Student	$250	$250
Primer Course 1+2	$350	$350
Primer Course Student	$200	$200
Additional Items		
Guest Opening Cocktail Reception Ticket	$40	$40
Guest Exhibition Opening Reception Ticket	$80	$80
Adtl. Digest USB	$100	$100
Adtl. Short Course USB	$100	$100
Adtl. Primer Course Notes USB	$100	$100
Adtl. Full Access Exhibitor Registration	$295	$295
Adtl. Exhibits Only Registration	$195	$195

All fees are denominated in US$
Full Registration Includes: USB, eBook, all refreshments Monday - Wednesday, continental breakfast Monday - Wednesday, Sunday Reception, Monday Reception, Tuesday Lunch.
Short Course Registration Includes: Short Course Notes on USB, continental breakfast and Short Course Lunch
[1]One-day Registration Includes: USB only (no social functions)
Primer Course Registration includes: Primer Course Notes on USB Only

For **ADVANCE REGISTRATION,** click on the Symposium Registration link on the Symposium website (www.csics.org). Please note that advance registration ends on September 23rd.

For registration and payment related questions, please contact:

IEEE/MCM: Brianna Hunt, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-844-816-1739
Fax : +1-609-689-0069
Email: csicsreg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency or traveler's checks. Checks must be made payable to "IEEE/2016 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

When you register for the Conference, the contact information you provide (including your name, address, phone, and email address) may be shared with CSICS and, with your explicit consent, vendor exhibitors.

We urge you to pre-register to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

Registration Center:

The Symposium Registration Center is located in the Prefunction Area on Sunday, Monday, Tuesday & Wednesday. The operating hours will be as follows:

Short & Primer Course Registration only

Sunday, October 23rd	7:00 a.m. – 8:00 a.m. Prefunction Area

Symposium Registration

Sunday, October 23rd	3:00 p.m. – 8:00 p.m. Prefunction Area
Monday, October 24th	7:00 a.m. – 5:00 p.m. Prefunction Area
Tuesday, October 25th	7:00 a.m. – 5:00 p.m. Prefunction Area
Wednesday, October 26th	7:00 a.m. – 12:00 p.m. Prefunction Area

Refund Policy:

All requests for refund/cancellation must be received in writing by September 23rd, 2016. No refunds can be provided after this date. Cancellations will incur a US$50 administration fee. Please submit cancellation requests via email to csicsreg@ieee.org

ACCOMMODATIONS

Hotel Reservations:

A block of rooms has been reserved at special discounted rates for Symposium participants at our headquarters hotel, the Doubletree by Hilton Hotel Austin. This hotel offers the very best in comfort and in service, from guest rooms to meeting rooms. Situated between the downtown business district and the Austin Arboretum, this north Austin hotel is just 20 minutes from Austin Bergstrom International Airport and five minutes from downtown Austin. Our elegant Spanish Colonial-style Austin, Texas hotel is minutes from the best shopping, dining and entertainment Austin has to offer.

Hotel Address and Phone Numbers:

DoubleTree by Hilton Hotel Austin
6505 N Interstate 35, Austin, Texas, 78752-4346, USA
TEL: +1-512-454-3737
FAX: +1-512-454-6915
Web Site: http://doubletree3.hilton.com/en/hotels/texas/doubletree-by-hilton-hotel-austin

While there are alternatives, we would like to remind attendees to please support the Symposium and fully enjoy all the activities by staying at the official headquarters hotel. The Symposium relies on attendees staying at the conference Hotel to reduce the costs charged for the use of meeting rooms. Room reservations should be made as soon as possible, as there are a limited number available at the symposium rate. **To qualify for the discounted rate reservations must be made by October 1, 2016**. Rooms are available at the special Symposium group rate of US$179 plus tax (15.75%) per night. Rates are for single occupancy. An extra person charge per person may apply for 2 or more guests sharing the same guestroom.

If you wish to cancel, please do so 24 hours before arrival to avoid cancellation penalties.

To make a reservation, you can follow the link on the symposium website or contact the hotel direct at +1-512-454-3737and ask for Reservations. Be certain to request the Special Group Rate for the IEEE CSIC Symposium or reserve on-line at:

http://doubletree.hilton.com/en/dt/groups/personalized/A/AUSLNDT-CSI-20161021/index.jhtml?WT.mc_id=PO G

Rooms will be subject to availability and possibly be charged at higher rates. Check-in time is 3 p.m. or later; check-out time is 12 noon. If necessary, you may cancel your reservation 24 hours prior to arrival to avoid cancellation penalties

TRANSPORTATION

Travel Arrangements:

Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc. by calling between the hours of 8:00 a.m. and 5:30 p.m. EST Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 717 556 1100. Or, you may visit their on-line travel service web site at http://www.ieee.org/travel. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Or you can e-mail your request to ieee@worldtravelinc.com.

IEEE corporate car rental discounts are also available to all attendees of the symposium. Discount codes below entitle attendees to receive special rates that have also been negotiated with Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.

Airport Transportation:

The Austin-Bergstrom International Airport (AUS) is about 12 miles from the Double Tree by Hilton Hotel Austin Orleans. The airport accommodates domestic and international travel.

Airport Transfer:

Super Shuttle (typical minimum charge, 17.00 USD) Airport Reservations: 1-800-BLUE VAN (258-3826)

http://www.supershuttle.com/Locations/AUSAirportShuttleAustin.aspx

Taxi: the typical minimum charge from AUS to the hotel is 30.00 USD.

Yellow Cab: 512-452-9999
Austin Cab: 512-478-2222
Lone Star Cab: 512-836-4900

Driving Directions:

From Airport, turn west (left) onto Hwy 71/Ben White Blvd.
Take Hwy 183 North to Hwy 290 West.
Take Hwy 290 West to the IH35 exit.
Turn right (north) on the access road..
The hotel is 2 blocks north on right.

ADDITIONAL INFORMATION

Distribution of Relevant Information:

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to be indiscriminately proliferated in the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition.

Photography:

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. No flash photography will be used. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE. Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.

Non Discrimination Policy

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws. For more information on the IEEE policy visit:

http://www.ieee.org/about/corporate/governance/p9-26.html?WT.mc_id=hpf_pol

Breakfast and Lunch Locations:

Breakfasts:

The location of breakfasts will be as follows:

Short Course + Primer Registrants (only) –
Sunday, October 23rd Dewitt

Symposium Registrants –
Monday, October 24th: Dovers
Tuesday, October 25th: Phoenix South
Wednesday, October 26th: Phoenix South

Lunches:

The location of lunches will be as follows:

Short Course + Primer Registrants (only) –
Sunday, October 23rd: Dewitt

Exhibition Luncheon –
Tuesday, October 25th: Phoenix South

Coffee Breaks:

The location of coffee breaks will be as follows:

Short Course and Primer registrants (only) –
Sunday, October 23rd: Prefunction Area

Symposium Registrants –
Monday, October 24th: Prefunction Area
Tuesday, October 25th: Prefunction Area
Wednesday, October 26th: Prefunction Area

Symposium Social Events:

SYMPOSIUM Opening Cocktail

We welcome you to Austin on Sunday evening, October 23rd from 7:00 p.m. to 8:00 p.m. in the Dovers room of the Doubletree by Hilton Hotel Austin. Come and meet up with your old friends and make new acquaintances over cheese and wine, beer or soft drinks. One free admission is included with your registration including two drink tickets, and extra reception tickets may be purchased at registration for $40.

EXHIBITION OPENING RECEPTION

The exhibition opening reception will be held on Monday evening, October 24th from 6:00 p.m. to 7:30 p.m. in the Phoenix South/Central Ballroom of the Doubletree by Hilton Hotel Austin. Come along; visit with the exhibitors over light hors d'oeuvres and wine, beer, or soft drinks. One free admission is included with your registration, and extra reception tickets may be purchased at registration for $80.

EXHIBITION LUNCHEON

On Tuesday, October 25th at noon the Exhibition Luncheon will be hosted in the Phoenix South Ballroom. The lunch is free to all Symposium participants, so come along, visit with the exhibitors, ask questions, make deals and find out what is going on in our industry.

Austin Attractions:

Located in Central Texas on the eastern edge of the American Southwest, Austin is the fourth-largest city in Texas and the 15th-largest in the United States. It was the third-fastest growing large city in the nation from 2000 to 2006. Residents of Austin are known as "Austinites" and include a diverse mix of university professors, students, politicians, musicians, state employees, high-tech workers, blue-collar workers, and white-collar workers. The main campus of the University of Texas is located in Austin. The city is home to development centers for many technology corporations and has adopted the nickname "Silicon Hills" due to its location on the eastern edge of hill country. Additionally, the city's official slogan promotes it as "The Live Music Capital of the World", a reference to the many musicians and live music venues within the area. Austin is also a center for film and home to the University of Texas and Formula 1's Circuit of the Americas raceway. Its abundant parks and lakes are popular for hiking, biking, swimming, boating and other outdoor pursuits. Austin is home to a wonderful ballet, world-class museums, one-of-a-kind shopping and beautiful outdoor spaces. You can just as easily spend your morning paddling the lake as you can strolling through a celebrated history museum.

Austin Weather:

October in Austin brings an average high of 80°F (27°C) and an average low of 58°F (15°C).

SYMPOSIUM HIGHLIGHTS

The technical program for the 2016 IEEE CSIC Symposium consists of 63 technical papers, three panel sessions, an industry exhibit, and two short courses: "Terahertz SiGe HBT technologies: Creating the winning design engine" and "GaN and SiC technologies for Power Electronics" We will also be offering two primer level classes: "Introduction to Si RFIC Design" and "Fundamentals of A/D Converters".

This year we have invited 26 papers on a wide range of important topics encompassing advanced device engineering to circuit application using compound and other related semiconductor technologies.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. This year there is considerable interest and papers in high power GaN on Diamond, Advanced Optical Front Ends, Next Generation devices, reconfigurable RF components, High Frequency device modeling, Silicon Photonics, and THz systems.. As always there is a tremendous amount of activity in wireless communications and military electronics.

Late-Breaking News Papers:

We have 13 late-breaking news papers. These will be presented in Session J starting at 3:30 p.m. on Tuesday October 25th and in sessions R and S starting at 3:30 p.m. on Wednesday October 26th.

Technical Digest:

Extra USB Technical Digests can be purchased by Symposium registrants through Advance Registration. A limited number of Digests USBs may also be available for sale at the Registration Desk. The cost of the USB ordered through Advance Registration or purchased on-site is $100.

Outstanding Paper Award:

The 2016 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the session chairpersons. The award winner will be announced after this year's Symposium with the award being formally presented during the 2016 CSIC Symposium.

Student Paper Competition:

In recognition of the exceptional contributions made by students, CSICS is proud to hold its second annual Student Paper Competition. To participate in the competition, an eligible student must submit a regular contributed paper naming, at a minimum, themselves and their principal supervisor as authors. The Student Paper Finalists must present their own papers at their assigned symposium session. We congratulate our thirteen Student Paper Finalists for 2016 CSICS. The winner of the student paper competition will be announced at the beginning of Session R.

Short Course 1: "Terahertz SiGe HBT technologies: Creating the winning design engine"

Current advanced SiGe HBT BiCMOS processes enable a wide array of sub-mm-wave and emerging terahertz applications. These applications encompass many areas including health, material science, transportation safety, industrial automation, communications, and space exploration. To realize these high performance circuits and systems, advanced process and device technologies are essential. SiGe HBT BiCMOS technology is a good choice due to the combination of high speed HBT devices and the high integration levels of CMOS. This course demonstrates how terahertz SiGe HBT process technology advances, TCAD/numerical device simulation techniques, compact modeling, and RF circuit design techniques combine to realize terahertz circuits and systems. The first portion of the course will describe THz SiGe HBT device and process technology. The second portion will discuss how TCAD and numerical simulations are applied to enable high performance devices. The third portion will discuss compact modeling extraction and validation approaches for sub-mm-wave and terahertz applications. The fourth portion will discuss system requirements and the challenges of terahertz circuit design. Several application demonstration examples will be given.

Short Course 2: "GaN and SiC technologies for Power Electronics"

GaN and SiC have emerged as possible replacements for incumbent silicon power conversion electronics. The power semiconductors markets for both are growing rapidly. Both technologies are attractive for their ability to reduce system size and save energy through higher efficiencies. Some examples of potential applications where GaN and SiC can outperform silicon technologies include power factor correction, wireless power transmission, ultra-compact high frequency adapters, efficient small-size photovoltaic inverters, and network and server power supplies. This short course will cover SiC and GaN device technologies as well as some application examples. The first course section will discuss SiC power diodes, SiC power MOSFETs, and power modules from basic device maturity, reliability, and applications perspectives. Topics to be presented include: SiC historical progress and bulk wafer maturity, SiC power diodes from 600V to 10kV, SiC power MOSFETs from 650V to 10kV, applications using SiC, and future trends in SiC devices and applications. The second section will discuss Gallium Nitride (GaN) on Silicon HEMT power switch devices and modules. The maturity and reliability of the technology will be discussed.

Direct questions to:
Brian Moser, Short Courses Coordinator
Qorvo
+1 336.678.8573
brian.moser@qorvo.com

Panel Sessions:

This year we have three exciting Panel Sessions on Tuesday October 25th and Wednesday October 26th. These are intended to be timely, thought-provoking, educational, and hopefully controversial. The three panel topics are as follows:

PANEL SESSION 1:
III-V vs. Si-Photonic Integrated Circuits (PIC) - What will survive the future?
Tuesday, October 25th, 10:30 a.m. - 12:00 p.m.

PANEL SESSION 2:
THz Metrology and MMIC Testing: Capability, Availability, and Cost. What is its impact on the advancement and development of THz MMICs, systems, and applications?
Tuesday, October 25th, 5:30 p.m. - 7:00 p.m. (cash bar)

PANEL SESSION 3:
Reconfigurable RF Systems, Fact or Fiction?
Wednesday, October 26th, 12:00 p.m. - 1:30 p.m.

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to day and time).

Technology Exhibition

The 2016 IEEE CSICS Technology Exhibition will be held on Monday evening October 24th and Tuesday the 25th in the Pavilion and is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, as well as the latest information on modeling and design simulation tools. This year's exhibitors are:

Company Name	Booth #
Capitol Scientific/MMT	**23**
HRL Laboratories, LLC	**14**
Keysight Technologies	**43**
Maury Microwave	**45**
Microsanj, LLC	**47**
NI (Formerly AWR corp.)	**63**
Pico Technology	**55**
Presidio Components, Inc.	**53**
Silvaco	**65**
Sonnet Software	**25**
StratEdge Corp.	**33**
Tektronix	**16**
TMX Scientific Inc.	**71**
Virgina Diodes Inc.	**35**
Wolfspeed, a Cree Company	**73**

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 4:30 p.m. and 7:30 p.m. on Monday, October 24th, and between 7:00 a.m. and 3:30 p.m. on Tuesday, October 25th. The Exhibition will also host the Exhibition Opening Reception from 6:00 p.m. until 7:30 p.m. on Monday evening and the Exhibition Luncheon from 12:00 noon to 1:30 p.m. on Tuesday. The Exhibition Opening Reception, the Exhibition Luncheon, and the Tuesday coffee breaks will be held in the exhibition area in the Phoenix South Ballroom.

To participate in the Exhibition, please contact Candi Wooldridge (MP Associates), candi@mpassociates.com, (303) 530-4562. Please visit the Symposium website at www.csics.org for additional information.

Short Courses

Sunday, October 23rd, 2016
Doubletree by Hilton
Austin, TX

Course Coordinator: **Brian Moser**
Qorvo
+1 336.678.8573
brian.moser@qorvo.com

"Terahertz SiGe HBT technologies: Creating the winning design engine"
Austin 7:30 a.m. – 3:00 p.m.

The sub-millimeter wave to terahertz region of the electro-magnetic spectrum is being increasingly utilized for commercial and research applications. These applications encompass many fields such as health, material science, transportation safety, industrial automation, communications, and space exploration. To realize these high performance circuits and systems, advanced process and device technologies are essential. SiGe HBT BiCMOS technology is a good choice due to the combination of high speed HBT devices and the high integration levels of CMOS. This course demonstrates how terahertz SiGe HBT process technology advances, TCAD/numerical device simulation techniques, compact modeling, and RF circuit design techniques combine to realize terahertz system applications. The first course section discusses the advances in device architecture and process technology that enable SiGe HBTs with maximum oscillation frequencies (fmax) up to 700GHz. One device challenge is the formation of a low-ohmic link between the intrinsic base and the base contact in a compatible way with lateral and vertical device scaling. Device optimization approaches are discussed to overcome major limitations of widely used SiGe HBT technologies. One example is double-polysilicon self-aligned (DPSA) selective epitaxial growth (SEG) technology. Another HBT fabrication challenge is aggressively scaled doping profiles for very short transit times. The impact of profile scaling on DC and RF transistor characteristics will be discussed. The second course section reviews the widely used drift-diffusion (DD) and hydrodynamic (HD) transport models available in most commercial and academic device simulators with an emphasis on application to advanced SiGe HBT devices. Since both the DD and the HD transport model can be derived from the Boltzmann transport equation (BTE), the results obtained by DD/HD are compared with BTE results and available experimental data. Compared to DD/HD, the computational cost of a deterministic BTE solver is currently much more expensive, making those methods less suitable for the everyday engineering work. To enable shorter simulation times and keep DD/HD predictive capability, strategies are described for tuning DD/HD with respect to BTE terminal characteristics such as the transfer characteristics or transit frequency fT. Examples of DD/HD and BTE terminal characteristic differences will be discussed such as fT differences originating from unsuitable representations of the doping/germanium profile. The third section gives a brief overview on the most relevant physical effects in high-speed SiGe HBTs. The associated compact

formulations and their integration in an advanced compact model will be presented. Next, the procedure for an independent as possible determination of the model parameters will be discussed with an emphasis on generating physics-based, geometry scalable large-signal compact models. Selected examples will be provided for extraction steps, related results, and a comparison between model and experimental data for the most advanced process technology SiGe HBT devices. Further model verification will be demonstrated by comparing simulation and measured data of various mm-wave benchmark circuits. Finally, major issues regarding reliable compact modeling, parameter extraction, and measurement capability will be discussed. The fourth section discusses the challenges and opportunities for emerging applications and circuit innovations. Recent attempts to operate SiGe HBTs close to and beyond their transistor cut-off frequencies will be presented. Silicon process technologies with an fmax above 0.5 THz enable circuits to operate fundamentally up to about 240 GHz with reasonable RF circuit performance. Beyond fmax, where transistors do not provide power gain, circuits may be operated sub- harmonically to extend the useful operation region. Both fundamental and sub-harmonic RF circuit design methodologies will be discussed. At THz frequencies, on-chip antennas may be implemented with reasonably high efficiencies and very small area, thus eliminating additional external components such as expensive waveguides or horn antennas. Other topics presented include RF power generation techniques beyond 300 GHz and circuit modeling and characterization methodologies up to 1 THz. Application demonstration examples include: communication towards 100 Gbit/s at 240 GHz, circular polarized radar transceivers for 3D imaging at 240 GHz, multi-color imaging up to 1 THz/video camera design up to 4 THz, incoherent SiGe sources with 0dBm up to 0.5 THz, and THz near-field imaging beyond the diffraction barrier.

Topics Covered and Instructors:

1) Terahertz SiGe HBT Process Technology – Dr. Holger Ruecker (IHP)

2) Terahertz SiGe HBT TCAD and numerical device simulation – Dipl.-Ing. Gerald Wedel (TU Dresden)

3) Compact modeling for mm- and sub-mm-wave applications - Prof. Michael Schroter (TU Dresden/UCSD)

4) From Terahertz Systems to RF Circuit Design – Prof. Ullrich Pfeiffer (U. Wuppertal)

"GaN and SiC technologies for Power Electronics" Austin 3:00 p.m. – 7:00 p.m.

GaN and SiC have emerged as possible replacements for incumbent silicon power conversion electronics. The power semiconductors markets for both are growing rapidly. Both technologies are attractive for their ability to reduce system size and save energy through higher efficiencies. Some examples of potential applications where GaN and SiC can outperform silicon technologies include power factor correction, wireless power transmission, ultra-compact high frequency adapters, efficient small-size photovoltaic inverters, and network and server power supplies. This short course will cover SiC and GaN device technologies as well as some application examples. The first course section will discuss SiC power diodes, SiC power MOSFETs, and power modules from basic device maturity, reliability, and applications perspectives. Topics to be presented include: SiC historical progress and bulk wafer maturity, SiC power diodes from 600V to 10kV, SiC power MOSFETs from 650V to 10kV, applications using

SiC, and future trends in SiC devices and applications. The second section will discuss Gallium Nitride (GaN) on Silicon HEMT power switch devices and modules. The maturity and reliability of the technology will be discussed. The course is presented by Dr. Jeffrey B. Casady, and Dr. Primit Parikh, both renowned experts in their fields

Topics Covered and Instructors:
1) Technical and reliability maturity of SiC power diodes, MOSFETs, and modules in 2016 – Dr. Jeffrey B. Casady (Wolfspeed)
2) GaN power devices and process - Dr. Primit Parikh (Transphorm)

Short Course Schedule

The short courses are held on Sunday October 23rd in the Austin room. A continental breakfast is available to all registered Short Course attendees and instructors. The first course "Terahertz SiGe HBT technologies: Creating the winning design engine" will begin at 7:30am and finish at 2:30 pm. A lunch will be provided as well as morning and afternoon refreshment breaks.

The second short course "GaN and SiC technologies for Power Electronics" will begin at 3:00 pm and finish at 7:00 pm and includes a refreshment break. All participants are invited to join the Symposium Opening Reception at 7:00 pm in the Dovers room.

Short Course I – Terahertz SiGe HBT technologies: Creating the winning design engine

Austin

7:00 a.m.	**Registration and Breakfast**
7:30 a.m.	**Introduction and Overview**
7:45 a.m.	**Terahertz SiGe HBT Process Technology** Dr. Holger Ruecker (IHP)
9:00 a.m.	**Terahertz SiGe HBT TCAD and numerical device simulation** Dipl.-Ing. Gerald Wedel (TU Dresden)
10:15 a.m.	**Coffee Break**
10:45 a.m.	**Compact modeling for mm- and sub-mm-wave applications** Prof. Michael Schroter (TU Dresden/UCSD)
12:00 p.m.	**Lunch**
1:00 p.m.	**From Terahertz Systems to RF Circuit Design** Prof. Ullrich Pfeiffer (U. Wuppertal)
2:15 p.m.	**Coffee Break and Q&A**
2:30 p.m.	**Close of Short Course**

Short Course II - GaN and SiC technologies for Power Electronics

Austin

2:00 p.m.	**Registration**
3:00 p.m.	**Introduction and Overview**
3:15 p.m.	**Technical and reliability maturity of SiC power diodes, MOSFETs, and modules in 2016** Dr. Jeffrey B. Casady (Wolfspeed)
4:45 p.m.	**Coffee Break**
5:15 p.m.	**GaN power devices and process** Dr. Primit Parikh (Transphorm)
6:45 p.m.	**Questions and Discussion**
7:00 p.m.	**Close of Short Course**

Who Should Attend

The first short course is aimed towards technologists and design engineers who would like to gain a better overall understanding of advanced SiGe BiCMOS technologies and the methods for successful sub-mm wave and terahertz design with SiGe BiCMOS. It is designed to review THZ SiGe HBT process technology advances, TCAD/numerical HBT device simulation, compact modeling for mm- and sub-mm-wave, and THz RF circuit design and systems.

The second course is intended for technologists or design engineers who are interested in learning more about the power electronic improvements offered by high breakdown (≥600V) GaN and SiC technologies. SiC and GaN power device technology maturity will be discussed along with some design and application examples.

Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for the Short Courses. A limited number of Short Course registrations will be available on site Sunday October 23rd 7:00 am – 8:00 am. The registration fee for Short Course I and II is US$500 for professionals and US$250 for students. This includes attending the lectures, notes for both Short Courses on a USB stick, a continental breakfast, a lunch and morning/afternoon refreshments during breaks. Additional copies of the Short Course and Primer Notes on USB may be purchased for US$100 each.

Primer Courses

Sunday, October 23rd in Robertson
8:00 a.m. – 5:30 p.m.

Primer Course I - Introduction to Si RFIC Design

Instructor: Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Course Objective and Description:

Silicon Radio Frequency Integrated Circuits (RFICs) are the dominant technology for wireless transceivers and sensors due to their low cost, ease of integration with digital functions, and excellent RF performance. This course is intended for semiconductor professionals of all technical backgrounds who wish to learn or refresh their understanding of the fundamentals of designing the principal circuit building blocks in radio and radar SoCs. The primer will begin with an overview of the nanoscale CMOS transistors and integrated passives from an RF perspective, analyzing key concepts in device modeling and noise behavior. This will be followed by a comparison to SiGe and III-V transistor design. In so doing, the intent is to provide guidance on how the circuit design process differs and to enlighten attendees on subjects such as transistor sizing, proper layout practices, parasitic reduction strategies and transceiver integration. In the second part of the primer, the focus will shift to the key building blocks that make up Silicon based integrated transceivers. Among the blocks to be covered are LNAs, Mixers and VCOs. For each one, designers are confronted with a variety of different circuit topologies, each with its attendant strengths and performance metrics. Making the right choice very much depends on having an awareness of what the options are, good specmanship and how the block will affect overall transceiver performance. Finally, the course will provide examples of circuit blocks implemented in CMOS technology.

The course instructor, Dr. Waleed Khalil, is currently serving as an Associate professor at the ECE department and the ElectroScience Lab, The Ohio State University. Prior to joining Ohio State, Prof. Khalil spent 16 years at Intel Corporation where he held various technical and leadership positions in wireless and wireline communication groups. While at Intel, he established Intel's first analog device modeling methodology for mixed signal circuit design and also contributed to the development of Intel's first RF process technology. Prof. Khalil's current research areas of interest include: RF and mm-wave circuits and systems, sub-THz circuits, front-end actives and passives, high performance clocking circuits, GHz A/D and D/A circuits.

Primer I Agenda:

7:00 A.M.	**Breakfast**
8:00 A.M.	**Introduction and Overview**
8:15 A.M.	**CMOS RFIC technology Perspective: Active and Passive Device Modeling**
9:30 A.M.	**Coffee Break**
11:00 A.M.	**RF CMOS Block Level Design Fundamentals and Examples**
12:00-1:00 P.M.	**Lunch**

Primer Course II – Fundamentals of A/D Converters

Instructor: Dr Hui Pan
Broadcom Limited
Irvine, CA

Course Objective and Description:

As RF/IF sampling, software defined radio (SDR), Full-Band Capture (FBC), and Electronic Dispersion Compensation (EDC) have become reality in nanoscale CMOS technology, RF circuits and optical components are increasingly being replaced by digital signal processors (DSPs). As a result, understanding the principles and design of data converters has taken on much greater significance for RF and optical engineers. For those new to the subject, the learning curve is a steep one, because there are very distinct differences between continuous-time RFIC/MMIC circuits and discrete-time data converters. Even for experienced data converter designers, it can be a major challenge to make the best choice of architecture and circuits, when there are so many options. This primer on A/D converters (ADC) aims to lower the barrier to entry for newcomers, while providing new angles for incumbent practitioners by deriving the ADC fundamentals in a logical and unified framework. The course opens with a survey of the latest developments in ADC applications and a brief theory on sampling and quantization, followed by a systematic derivation of quantizers from basic search algorithms to various architecture and circuit implementations. Implementation imperfections and their impacts, remedies, and characterizations are covered in dedicated Sections. The course concludes with examples of using the derived principles to evaluate real ADC designs.

The course instructor, Doctor Hui Pan, is currently focusing on high performance data converter design at Broadcom Limited. He was a Technical Director and Distinguished Engineer of Broadcom Corporation responsible for developing high speed wireline communication circuits and systems. He received the B.E. degree from Tsinghua University, Beijing, China, in 1983 and the Ph.D. degree from UCLA in 1999. He was the recipient of the 1998 Analog Devices Outstanding Student Designer Award and the 2000 DAC Design Contest Honorable Mention for his work on an IF sampling ADC. Dr. Pan served on ISSCC TPC 2006 – 2010.

Primer II Agenda:

1:00 P.M.	**Applications and Systems**
1:30 P.M.	**Algorithms and Architectures**
2:30 P.M.	**Circuit Implementations**
3:00 P.M.	**Coffee Break**
3:30 P.M.	**Imperfections and Remedies**
4:30 P.M.	**Metrics and Measurements**
5:00 P.M.	**Design Examples**
5:30 P.M.	**Close of Primer II**

Primer Course Coordinator:
Bruce Green
NXP Semiconductors
1300 North Alma School Road, Chandler, AZ, 85224, USA
(480) 814-4360
Bruce.Green@nxp.com

Student Paper Finalists

Competition Chair: Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Presentation Schedule for the eight Student Paper Finalists:

Monday October 24, 2:20 p.m. (Phoenix North)

B.3 **Integrated Dual-Channel X-Band Offset-Transmitter for Phase Steering and DDMA Arrays**
Johan C. J. G. Withagen[1], A. J. Annema[1], B. Nauta[1], F. E. van Vliet[1,2]
[1]University of Twente, Enschede, The Netherlands
[2]TNO, The Hague, The Netherlands

Monday October 24, 2:40 p.m. (Phoenix North)

B.4 **A Wide-Band Complimentary Digital Driver for Pulse Modulated Single-Ended and Differential S/C Bands Class-E PAs in 130 nm GaAs Technology**
S. Rashid[1], B. Dupaix[1], T. Quach[2], P. Watson[2], W. Gaber[1], V. Patel[2], A. Mattamana[2], S. Dooley[2], M. LaRue[1], and W. Khalil[1]
[1]The Ohio State University, Columbus, USA
[2]Air Force Research Laboratory, WPAFB, USA

Monday October 24, 4:30 p.m. (Austin)

E.3 **Interconnect Technologies for Terabit-per-second Die-to-Die Interfaces**
B. Dehlaghi[1], R. Beerkens[2], D. Tonietto[2], A. Chan Carusone[1]
[1]University of Toronto, Toronto, Canada, [2]Huawei Canada Research Centre, Ottawa, Canada

Tuesday October 25, 2:20 p.m. (Austin)

H.3 **Digital Clock and Data Recovery Circuits for Optical Links**
G. Shu, W. Choi, P. K. Hanumolu,
University of Illinois, Urbana , United States

Tuesday October 25, 2:40 p.m. (Austin)

H.4 **A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS**
A. Roshan-Zamir, O. Elhadidy, H. Yang, S. Palermo, Texas A&M University, College Station, United States

Tuesday October 25, 2:20 p.m. (Phoenix North)

I.3 **A 14-GHz, 22-dBm Series Doherty Power Amplifier in 45-nm CMOS SOI**
C. S. Levy[1], V. Vorapipat[1], J. F. Buckwalter[2], [1]*University of California San Diego, La Jolla, USA*, [2]*University of California Santa Barbara, Santa Barbara, USA*

Wednesday October 26, 9:20 a.m. (Austin)

M.3 **A 20-Gbit/s RFDAC-based Direct-Modulation W-band Transmitter in 32-nm SOI CMOS**
H. Al-Rubaye, G. Rebeiz, *Dept. of Electrical and Computer Engineering, UC San Diego, United States*

Wednesday October 26, 2:00 p.m. (Phoenix North)

P.2 **Low Power Ultra-Wide Band LNA based on Active Impedance Matching Technique for UWB Wireless Communication**
Mantas Sakalas, P. Sakalas, F. Ellinger
Technische Universität, Dresden, Germany

CSIC Symposium Opening Cocktail Hour

Dovers

7:00 p.m. - 8:00 p.m.

SYMPOSIUM PROGRAM

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Prefunction Area – Doubletree by Hilton, Austin
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Dovers

SYMPOSIUM OPENING

8:30 a.m. – 9:00 a.m.
Phoenix North – Doubletree by Hilton, Austin

Opening Remarks
2016 Symposium General Chair
Harris P. Moyer, *HRL Laboratories*

MTT Co-Sponsor Message
Dylan Williams, NIST and President Elect of the MTT Society

Technical Program Overview
2016 Technical Program Chair
Jim Carroll, NI – AWR Group

SESSION A: PLENARY SESSION

9:00 a.m. – 12:00 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Brian Moser, *Qorvo*
Peter Zampardi, *Qorvo*

9:00 a.m.
A.1 **Towards Next Generations of Silicon Photonics (Invited)**
S. Cremer, C. Baudot, N. Vulliet, J. Durel, C. Durand, H. Petiton, E. Temporiti, F. Boeuf, *STMicroelectronics, Crolles, France*

9:30 a.m.
A.2 **Reconfigurable Electronics for Adaptive RF Systems (Invited)**
R. H. Olsson III[1], K. Bunch[2], C. Gordon[2], [1]*DARPA Arlington, United States*, [2]*Booz Allen Hamilton, Arlington, United States*

10:00 a.m. – 10:15 a.m.
Coffee Break

Monday, October 24th, 2016

10:15 a.m.

A.3 **The EU DOTSEVEN project: Overview and Results (Invited)**
M. Schroter[1,2], J. Boeck[3], V. d'Alessandro[4], S. Fregonese[5], B. Heinemann[6], C. Jungemann[7], W. Liang[1], H. Kamrani[7], A. Mukherjee[1], A. Pawlak[1], U. Pfeiffer[8], N. Rinaldi[4], N. Sarmah[8], T. Zimmer[5], *[1]Technical University Dresden, Germany, [2] UC San Diego, La Jolla, United States, [3]Infineon Technologies, Munich, Germany, [4]University Federico II, Naples, Italy, [5]IMS, University Bordeaux, France, [6]IHP, Frankfurt, Germany, [7]RWTH Aachen, Germany, [8]IHTC, University Wuppertal, Germany*

10:45 a.m.

A.4 **Advanced Antenna Architectures for THz Sensing Instruments (Invited)**
A. Neto, *Delft University of Technology, Delft, The Netherlands*

11:15 a.m.

A.5 **Millimeter Wave: The Future of Commercial Wireless Systems (Invited)**
R. W. Heath Jr., *The University of Texas at Austin, Austin, United States*

11:45 a.m.
End of Session A

12:00 p.m. – 1:30 p.m.
Break for Lunch

Monday, October 24th, 2016

SESSION B: Reconfigurable RF Components and Systems

1:30 p.m. – 3:00 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Tony Quach, *Air Force Research Laboratory*
Nabil El-Hinnawy, *Northrop Grumman Mission Systems*

1:30 p.m.
B.1 **Reconfigurable RF Components for Multifunction RF Systems (Invited)**
Stephen Hary[1], Taylor Barton[2]
[1]Air Force Research Laboratory, WPAFB, USA
[2]University of Colorado at Boulder, Boulder, USA

2:00 p.m.
B.2 **Multi-octave and Frequency-agile LNAs Covering S-C Band using 0.25 µm GaN Technology**
A. Mattamana[1], W. Gouty[1], W. Khalil[2], T. Quach[1], and P. Watson[1], V. J. Patel[1]
[1]Air Force Research Laboratory, WPAFB, USA,
[2]The Ohio State University, Columbus, USA

2:20 p.m.
B.3 **Integrated Dual-Channel X-Band Offset-Transmitter for Phase Steering and DDMA Arrays**
Johan C. J. G. Withagen[1], A. J. Annema[1], B. Nauta[1], F. E. van Vliet[1,2]
[1]University of Twente, Enschede, The Netherlands
[2]TNO, The Hague, The Netherlands

2:40 p.m.
B.4 **A Wide-Band Complimentary Digital Driver for Pulse Modulated Single-Ended and Differential S/C Bands Class-E PAs in 130 nm GaAs Technology**
S. Rashid[1], B. Dupaix[1], T. Quach[2], P. Watson[2], W. Gaber[1], V. Patel[2], A. Mattamana[2], S. Dooley[2], M. LaRue[1], and W. Khalil[1]
[1]The Ohio State University, Columbus, USA
[2]Air Force Research Laboratory, WPAFB, USA

3:00 p.m.
End of Session B

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION C: GaN HEMT Physical Characterization

1:30 p.m. – 3:00 p.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Tomoya Kaneko, *NEC*
Robert Howell, *Northrop Grumman*

1:30 p.m.
C.1 **Mechanism of Current-Collapse-Free Operation in E-mode GaN Gate Injection Transistors Employed for Efficient Power Conversion (Invited)**
K. Tanaka, T. Morita, H. Umeda, S. Tamura, H. Ishida, M. Ishida and T. Ueda, *Panasonic, Kyoto, Japan*

2:00 p.m.
C.2 **Electron Mobility and Self-Heat Modeling of AlN/GaN MIS-HEMTs with Embedded Source Field-Plate Structures**
H. Aoki[1], N. Tsukiji[1], H. Sakairi[2], K. Chikamatsu[2], N. Kuroda[2], S. Shibuya[1], K. Kurihara[1], M. Higashino[1], H. Kobayashi[1] and K. Nakahara[2], [1]*Gunma University, Kiryu-Shi, Japan;* [2]*ROHM Co, Kyoto, Japan*

2:20 p.m.
C.3 **Time Resolved Micro-beam X-ray Absorption Fine Structure (XAFS) Measurement to Investigate the Cause of a Current Collapse of GaN-HEMTs**
Y. Tateno[1], T. Kouchi[1], T. Komatani[2], H. Yamamoto[2], T. Yonemura[1], J. Iihara[1], Y. Saito[1], and T. Nakabayashi[1], [1]*Sumitomo Electric Industries, Yokohama, Japan,* [2]*Sumitomo Electric Device Innovations, Nakakoma-gun, Japan*

2:40 p.m.
End of Session C

3:00 p.m. – 3:30 p.m.
Coffee Break

Monday, October 24th, 2016

SESSION D: Millimeter-wave Circuits Using State-of-the-Art Transistors

3:30 p.m. – 5:00 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Kazuya Yamamoto, *Mitsubishi Electric*
Marc Rocci, *OMMIC*

3:30 p.m.
D.1 **SiGe Technology as a Millimeter-wave Platform: Scaling Issues, Reliability Physics, Circuit Performance, and New Opportunities (Invited)**
J. Cressler, C. Coen, S. Zeinolabedinzadeh, P. Song, R. Schmid, M. Oakley, P. Chakraborty, *Georgia Institute of Technology, Altanta, United States*

4:00 p.m.
D.2 **Ka-Band LNA MMIC's Realized in f_{max} > 580-GHz GaN HEMT Technology**
M. Micovic, D. Brown, D. Regan, J. Wong, J Tai, A. Kurdoghlian, F. Herrault, Y. Tang, S. Burnham, H. Fung, Adele Schmitz, I Khalaf, D. Santos, E. Prophet, H. Bracamontes, C. McGuire, R. Grabar, *HRL Laboratories LLC, Malibu, United States*

4:20 p.m.
D.3 **Broadband E-band Power Amplifier MMIC Based On An AlGaN/GaN HEMT Technology with 30-dBm Output Power**
D. Schwantuschke, B-J Godejohann, S. Breuer, P. Bruckner, M. Mikulla, R. Quay, O. Ambacher, *Fraunhofer Institute for Applied Solid-State Physics, Freiburg, Germany*

4:40 p.m.
D.4 **6-W Ka Band Power Amplifier and 1.2-dB NF X-band Amplifier Using a 100-nm GaN/Si Process**
R. Leblanc, N. Ibeas, A. Gasmi, F. Auvray, J. Poulain, F. Lecourt, G. Dagher, P. Frijlink, *OMMIC SAS, Limeil Brevannes, France*

5:00 p.m.
End of Session D

SESSION E: Mixed-Signal Circuits and Interconnects for 100G+ Systems

3:30 p.m. – 5:00 p.m. Monday
Austin – Doubletree by Hilton, Austin TX

Chairpersons: Yuriy Greshishchev, *Ciena*
James Buckwalter, *UCSB*

3.30 p.m.
E.1 **CMOS ADCs Towards 100 GS/s and Beyond (Invited)**
L. Kull, D. Luu, P. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, A. Cevrero, I. Oezkaya, H. Yueksel, T. Toifl, *IBM Research - Zurich, Switzerland*

4:00 p.m.
E.2 **Analog and Mixed-Signal Millimeter-Wave SiGe BiCMOS Circuits: State of the Art and Future Scaling (Invited)**
S. P. Voinigescu, S. Shopov, J. Hoffman, K. Vasilakopoulos, *University of Toronto, Toronto, Canada*

4:30 p.m.
E.3 **Interconnect Technologies for Terabit-per-second Die-to-Die Interfaces**
B. Dehlaghi[1], R. Beerkens[2], D. Tonietto[2], A. Chan Carusone[1]
[1]University of Toronto, Toronto, Canada, [2]Huawei Canada Research Centre, Ottawa, Canada

End of Session E

Technology Exhibition
Opening Reception
Phoenix South/Central Ballroom
5:30 p.m. - 7:30 p.m.

Tuesday, October 25th, 2016

REGISTRATION AND BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Prefunction Area
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Phoenix South

SESSION F: Broadband THz Systems and Applications

8:30 a.m. – 10:10 a.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: William Peatman**,** *II-VI, Inc.*
Zach Griffith, *Teledyne Scientific*

8:30 a.m.
F.1 **Terahertz Sources and Receivers for Science Applications and Test & Measurement Systems (Invited)**
T. Crowe, J. Hessler, E. Bryerton, S. Retzloff, *Virginia Diodes Inc (VDI), Charlottesville, United States*

9:00 a.m.
F.2 **Broadband GaN DHFET Traveling Wave Amplifiers with Up to 120-GHz Bandwidth**
D. Brown, A. Kurdoghlian, R. Grabar, D. Santos, J. Magadia, H. Fung, J. Tai, I Khalaf, M. Micovic, *HRL Laboratories LLC, Malibu United States*

9:20 a.m.
F.3 **Terahertz Detection and Imaging Systems and Applications (Invited)**
E. Grossman, J. Cheron, *National Institute of Standards and Technology (NIST), Boulder, United States*

9:50 a.m.
F.4 **Ultra-Wideband mm-Wave InP Power Amplifiers in 130-nm InP HBT Technology**
R. Maurer, S-K Kim, M. Urteaga*, M. Rodwell, *ECE Department, UC Santa Barbara, United States*
**Teledyne Scientific, Thousand Oaks, United States*

10:10 a.m.
End of Session F

10:00 a.m. – 10:30 a.m.
Coffee Break

SESSION G: GaN on Diamond

8:30 a.m. – 9:50 a.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Bruce Green, NXP Semiconductors
Avram Bar-Cohen, *University of Maryland*

8:30 a.m.
G.1 **Prospects for Gallium Nitride-on-Diamond Transistors**
J.D. Blevins, G.D. Via, *AFRL, Dayton, Ohio*

8:50 a.m.
G.2 **Characterization of the Thermal Conductivity of CVD Diamond for GaN-on-Diamond Devices**
L. Yates[1], A. Sood[2], Z. Cheng[1], T. Bougher[1], K. Malcolm[1], J. Cho[2], M. Asheghi[2], K. Goodson[2], M. Goorsky[3], F. Faili[4], D. Twitchen[4] and S. Graham[1], [1]*Georgia Institute of Technology, Atlanta, USA,* [2]*Stanford University, Stanford, USA,* [3]*UCLA, Los Angeles, USA,* [4]*Element Six Technologies, San Jose, USA.*

9:10 a.m.
G.3 **Investigation of Stresses in GaN HEMT Layers on a Diamond Substrate Using Micro-Raman Spectroscopy**
B. Logan Hancock, M. Nazari, J. Anderson, E. Piner and M. Holtz, *Texas State University, San Marcos, United States*

9:30 a.m.
G.4 **Elimination of Leakage in GaN-on-Diamond**
B. Alvarez[1], D. Francis[1], F. Faili[1], F. Lowe[1], D. Twitchen[1], K.B. Lee[2] and P. Houston[2], [1] *Element Six, Santa Clara, United State,* [2]*University of Sheffield, Sheffield, United Kingdom*

9:50 a.m.
End of Session G

10:00 a.m. – 10:30 a.m.
Coffee Break

Tuesday, October 25th, 2016

PANEL SESSION 1: III-V vs. Si-Photonic Integrated Circuits (PIC) - What will survive the future?

Phoenix – Doubletree by Hilton, Austin TX
Tuesday 10:30 AM

Moderators: Shahriar Shahramian, Nokia
Mark Webster, Cisco

III-V has been the main solution of optical communication systems. And III-V PIC's have been used in high-performance optical systems such as tunable DWDM and coherent optics for long-haul transport. Silicon Photonics has been showing significant progress in performance, manufacturability and cost reduction in the last few years. The area of growth has been in the 500m to 2km communication links, with PSM4 standardization. Recently there has been demonstration of Si PIC's in integrated coherent receiver. Both of these PIC technologies have their challenges with implementation, reach, power performance and cost. The question is, will III-V and Si PIC technologies coexist or one will dominate over the other. This panel is a fusion of tutorial, debate and open discussion on the topic. Our fine group of experts will present their views on the role of PICs and the questions posed. They will also engage the audience and respond to their questions or comments.

- What are the main characteristics of Si PIC that endanger III-V?
- What are the characteristics of III-V PIC that may secure their future?
- Do we expect new revolutionary transformations in III-V PIC that may impact Si PIC adoption?

Panel Members:

Sebastien Cremer	ST Microelectronics
Marco Fiorentino	Hewlett Packard Labs
Martin Guy	Ciena
The'Linh Nguyen	Finisar

12:00 p.m.
End of Panel Session 1

Technology Exhibition Lunch
Phoenix South Ballroom
12:00 p.m. – 1:30 p.m.

SESSION H: High-Speed Circuits for Optical and Electrical Links

1:30 p.m. – 3:00 p.m. Tuesday
Austin – Doubletree by Hilton, Austin

Chairpersons: Thé Linh Nguyen, *Finisar Corporation*
Cheng Li, *Hewlett Packard Labs*

1.30 p.m.
H.1 **70+Gb/s VCSEL-based Multimode Fiber Links (Invited)**
D. M. Kuchta[1], A. V. Rylyakov[2], F. E. Doany[1], C. L. Schow[3], J. E. Proesel[1], C. W. Baks[1], P. Westbergh[4], Gustavsson[5], A. Larsson[5]
[1]IBM , Yorktown Heights, United States, [2]Coriant Advanced Technology Group, New York, United States, [3]U. C. Santa Barbara, Santa Barbara, United States, [4]Finisar Corporation, Allen, United States, [5]Chalmers University of Technology, G¨oteborg, Sweden

2:00 p.m.
H.2 **A 45-mW 50-Gb/s Linear Shunt LD Driver in 0.5-um InP HBT Technology**
T. Kishi[1], M. Nagatani[1], S. Kanazawa[2], W. Kobayashi1, T. Shindo[1], H. Yamazaki[1], M. Ida[1], K. Kurishima[1], H. Nosaka[1]
[1]NTT Device Technology Laboratories, Atsugi-shi, Japan, [2]NTT Device Innovation Center, Atsugi-shi, Japan

2:20 p.m.
H.3 **Digital Clock and Data Recovery Circuits for Optical Links**
G. Shu, W. Choi, P. K. Hanumolu,
University of Illinois, Urbana , United States

2:40 p.m.
H.4 **A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS**
A. Roshan-Zamir, O. Elhadidy, H. Yang, S. Palermo, Texas A&M University, College Station, United States

3:00 p.m.
End of Session H

3:00 p.m. – 3:30 p.m.
Coffee Break

Tuesday, October 25th, 2016

SESSION I: High-Power Amplifier Technology

1:30 p.m. – 3:30 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Taylor Barton, *University of Colorado Boulder*
Jon Mooney, *Raytheon*

1:30 p.m.
I.1 **Microwave Transistor Power Rectifiers and Applications (Invited)**
Z. Popovic, I. Ramos, T. Reveyrand, M. Litchfield, *University of Colorado Boulder, Boulder USA*

2:00 p.m.
I.2 **X-Band GaN Multi-Level Chireix Outphasing PA with a Discrete Supply Modulator MMIC**
M. Litchfield[1], T. Cappello[2], C. Florian[2], Z. Popovic[1], [1]*University of Colorado Boulder, Boulder, USA,* [2]*University of Bologna, Bologna, Italy*

2:20 p.m.
I.3 **A 14-GHz, 22-dBm Series Doherty Power Amplifier in 45-nm CMOS SOI**
C. S. Levy[1], V. Vorapipat[1], J. F. Buckwalter[2], [1]*University of California San Diego, La Jolla, USA*, [2]*University of California Santa Barbara, Santa Barbara, USA*

2:40 p.m.
I.4 **High Efficiency 5W/10W 32 - 38GHz Power Amplifier MMICs Utilizing Advanced 0.15um GaN HEMT Technology**
S. Chen, S. Nayak, C. F. Campbell, E. Reese, *Qorvo, Richardson, USA*

3:00 p.m.
I.5 **Analysis of odd-mode parametric instabilities at fundamental frequency in an X-band MMIC Power Amplifier**
S. Dellier[1], L. Mori[2], J. Collantes[2], A. Anakabe[2], C. Campbell[3], [1]*AMCAD Engineering, Limoges, France,* [2]*University of the Basque Country, Bilbao, Spain,* [3]*Qorvo, Richardson, USA*

3:30 p.m.
End of Session I

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION J: Late-Breaking News I

3:30 p.m. – 5:00 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Pete Zampardi, *Qorvo*
Simon Wood, *Wolfspeed*

3:30 p.m.
J.1 **Suitability of InP DHBTs in ET/APT Systems**
P. J. Zampardi[1], B. Moser[2], J. C. Li[3], D. Gamini[2], D. Limanto[2], K. Muhonen[2], *[1]Qorvo, Newbury Park, United States, [2]Qorvo, Greensboro, United States, [3]HRL Laboratories, Malibu, United States*

3:50 p.m.
J.2 **A High Efficiency High Power Density Harmonic-tuned Ka Band Stacked-FET GaAs Power Amplifier**
D. P. Nguyen, T. Pham, B. L. Pham, A. Pham, *University of California, Davis, Davis, United States*

4:10 p.m.
J.3 **A 40 Gbps Micro-Ring Modulator Driver implemented in a SiGe BiCMOS Technology**
A. Fatemi[1], D. Kissinger[2], H. Klar[1], F. Gerfers[1], *[1]Chair of Mixed Signal Circuit Design, Berlin, Germany, [2]Innovations for High Performance Microelectronics, Frankfurt (Oder), Germany*

4:30 p.m.
J.4 **The Role of Measurement Uncertainty in Achieving First-Pass Design Success**
D. Williams[1], R. A. Chamberlin[1], W. Zhao[2], J. Cheron[1], M. Urteaga[3], *[1]National Institute of Standards and Technology, Boulder, United States, [2]Xidian University, Xi'an, China, [3]Teledyne Scientific, Thousand Oaks, United States*

4:50 p.m.
End of Session J

Tuesday, October 25th, 2016

SESSION K: Noise and Non-Linear Modeling

3:30 p.m. – 4:50 p.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Mikael Garcia, *Analog Devices*
Michael Schroter, *TU Dresden/UCSD*

3:30 p.m.
K.1 **Microwave Noise Analysis in InP and GaAs HBTs (Invited)**
P. Sakalas[1,2], T. Nardmann[1], A. Simukovic, M. Schroter[1,3], H. Zirath[4], [1]*Technische Universitat, Dresden, Germany,* [2]*FRL Semiconductor Physics Institute of Center of Physical Sciences and Technology, Vilnus, Lithuania,* [3]*University of California San Diego, La Jolla, United States,* [4]*Chalmers University of Technology, Gothenburg, Sweden.*

4:00 p.m.
K.2 **VNA Based Measurements and Nonlinear Modeling for Efficient RF Circuit Design (Invited)**
S. Dellier, A. Xiong, C. Charbonniaud, C. Maziere, C. Enguehard, T. Gasseling , *AMCAD Engineering, Limoges, France*

4:30 p.m.
K.3 **Distortion in Difference Frequency Under Two-Tone Signal Input Evaluated with Volterra Series Analysis**
K. Tamesue, T. Egawa and A. Wakejima, *Nagoya Institute of Technology, Nagoya, Japan*

4:50 p.m.
End of Session K

Tuesday, October 25th, 2016

PANEL SESSION 2: THz Metrology and MMIC Testing - Capability, Availability, and Cost. What is its impact on the advancement and development of THz MMICs, systems, and applications?

5:30 p.m. – 7:00 p.m.
Phoenix North – Doubletree by Hilton Hotel Austin

Moderators: Zach Griffith, *Teledyne Scientific Company*
Miro Micovic, *HRL Laboratories LLC*

Over the past 10 years, there have been significant increases to state-of-the-art frequency performance for InP HBT/HEMT, GaN HEMT, SiGe HBT, and Si-CMOS transistor technologies into the THz (greater than 0.3-THz) regime due to aggressive vertical and lateral scaling of the devices. While these devices have been getting faster, so has the computational power of computers running circuit design and electromagnetic simulation software. This now permits THz MMIC and system design to be accurately performed on significantly shorter timescales, thus allowing for more sophisticated modeling and design of THz circuits, antennas, radiometers, imagers, and communication links. Furthermore, THz metrology has made significant advancements as well; today vector network analyzer (VNA) characterization to 1.5-THz is now possible, as well as on-wafer waveguide coupled probe testing to 1.1-THz.

While there have been vast improvements to transistor bandwidth and the computational power of predictive simulations for THz design and chip realization, the metrology, packaging techniques, and testing methods used to characterize THz MMICs and systems has not changed much over this same time. This panel will debate the role and impact THz Metrology and MMIC testing is having on the advancement of THz MMICs, systems, and applications as they pertain to capability, availability, and cost. The debate will also consider the future prospects and opportunities for THz systems, and the other factors need to be addressed to increase their proliferation into the present application space, as well as discuss what opportunities that exist in the commercial arena.

Panel Members:

Tom Crowe	*VDI Inc*
Bill Deal	*Northrop Grumman (AS)*
Dylan Williams	*NIST*
Suren Singh	*Keysight Technologies*

7:00 p.m.
End of Panel Session 2

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 12:00 p.m.
Registration – Prefunction Area
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Phoenix South

SESSION L: GaN HEMT Modeling

8:30 a.m. – 9:50 a.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Subrata Halder, *Qorvo*
Parrish Ralston, *Northrop Grumman*

8:30 a.m.
L.1 **Physical Model of RF Leakage in GaN HEMTs on Si Substrates Based on Atomic Diffusion Analysis at Buffer/Substrate Interface**
Y. Yamaguchi[1], J. Kamioka[1], S. Shinjo[1], K. Yamanaka[1] and T. Oishi[2], [1]*Mitsubishi Electric Corporation, Kamakura, Japan,* [2]*Saga University, Saga, Japan*

8:50 a.m.
L.2 **Transient Thermal Response Impact of 3.5GHz GaN HEMT Amplifier on TDD LTE Spectrum and its Improvement Based on a Thermal Equivalent Circuit Approach**
T. Kaneko, K. Ohgami and Y. Murao, *NEC Corporation, Kanagawa, Japan*

9:10 a.m.
L.3 **The Impact of AlN Spacer on Forward Gate Current and Stress-Induced Leakage Current (SILC) of GaN HEMT**
C. Chen, D. Wang, D. Hou, Y. Yang, W. Yau, R. Sadler, W. Sutton, J. Shim and S. Wang, *Global Communication Semiconductos, Torrance, United States*

9:30 a.m.
L.4 **Compact Thermal Modeling of GaN HEMT Devices for Pulsed and CW Applications**
J. Liu[1], M. Calvo[1], L. Dunleavy[1], H. Morales[1], R. Martin[2], M. Woods[2] and N. Craig[2], [1]*Modelithics, Tampa, United State,* [2]*Qorvo, Richardson, United States*

9:50 a.m.
End of Session L

10:00 a.m. – 10:30 a.m.
Coffee Break

SESSION M: E- and W-band Technology and Circuits

8:30 a.m. – 10:00 a.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Herbert Knapp, *Infineon*
Miro Micovic, *HRL Laboratories*

8:30 a.m.
M.1 **Si-Based Technologies for mm-Wave Automotive Radar (Invited)**
J. John, J. Kirchgessner, R. Ma, D. Morgan, I. To, V. Trivedi, *NXP Semiconductors, Tempe, United States*

9:00 a.m.
M.2 **Ultra-low Power Components for a 94-GHz Transceiver**
S-K. Kim, R. Maurer, A. Simsek, *M. Urteaga, M. Rodwell, *ECE Department, UC Santa Barbara, United States*
**Teledyne Scientific, Thousand Oaks, United States*

9:20 a.m.
M.3 **A 20-Gbit/s RFDAC-based Direct-Modulation W-band Transmitter in 32-nm SOI CMOS**
H. Al-Rubaye, G. Rebeiz, *Dept. of Electrical and Computer Engineering, UC San Diego, United States*

9:40 a.m.
M.4 **35-nm InP HEMT LNAs at E/W-Band Frequencies**
N. Estrella, L Bui, E. Camargo, J. Schellenberg, *Quinstar Technology, Torrance, United States*

10:00 a.m.
End of Session M

10:00 a.m. – 10:30 a.m.
Coffee Break

SESSION N: High Power GaN

10:30 a.m. – 12:00 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Kazutaka Inoue, *Sumitomo Electric*
Ken Chu, *BAE*

10:30 a.m.
N.1 **High Power Density InAlGaN/GaN HEMT Technology for W-band Amplifiers (Invited)**
K. Makiyama[1,2,3], Y. Niida[1,2], S. Ozaki[1,2], T. Ohki[1,2], N. Okamoto[1,2], Y. Minoura[1,2], M. Sato[1,2], Y. Kamada[1,2], K. Joshin[1,2], K. Watanabe[1,2], and Y. Miyamoto[3], [1]*Fujitsu Limited,* [2]*Fujitsu Laboratories, Atsugi, Japan,* [3]*Tokyo Institute of Technology, Tokyo, Japan*

11:00 a.m.
N.2 **A GaN-based 10.1 MHz Class-F^{-1} 300W Continuous Wave Amplifier Targeting Industrial Power Applications**
F. Maier[1], D. Krausse[1], D. Gruner[1], R. Reiner[2], P. Waltereit[2], R. Quay[2], O. Ambacher[2], [1]*TRUMPF Huttinger GmbH & Co, Freiburg, Germany,* [2]*Fraunhofer Institute of Applied Solid State Physics, Freiburg, Germany*

11:20 a.m.
N.3 **650 V Highly Reliable GaN HEMTs on Si Substrates Over Multiple Generations-Matching Silicon CMOS Manufacturing Metrics and Process Control**
S. Chowdhury[1], Y. Wu[1], L. Shen[1], K. Smith[1], P. Smith[1], T. Kikkawa[1], J. Gritters[1], L. McCarthy[1], R. Lal[1], R. Barr[1], Z. Wang[1], U. Mishra[1], P. Parikh[1], T. Hosoda[2], K. Shono[2], K. Imanishi[2], T. Ogino[2], A. Mochizuki[2], K. Kiuchi[2] and Y. Asai[2], [1]*Transphorm, Goleta, United States,* [2]*Transphorm Japan, Aizu-Wakamatsu, Japan*

11:40 a.m.
N.4 **150V-Bias RF GaN for 1 kW UHF Radar Amplifiers**
G. Formicone, J. Burger and J. Custer, *Integra Technologies, El Segundo, United States*

12:00 p.m
End of Session N

12:00 p.m. – 1:30 p.m.
Break for Lunch

SESSION O: Components for Advanced Optical Front-End

10:30 a.m. – 12:00 p.m. Wednesday
Austin – Doubletree by Hilton, Austin TX

Chairpersons: Munehiko Nagatani, *NTT Corporation*
Craig Steinbeiser, *Qorvo*

10.30 a.m.
O.1 **InP Segmented Mach-Zehnder Modulators with Advanced Electro-Optical Functionalities (Invited)**
A. Aimone
Fraunhofer HHI, Berlin, Germany

11:00 a.m.
O.2 **A 56-Gb/s Transimpedance Amplifier in 0.13-um SiGe BiCMOS for an Optical Receiver with -18.8-dBm Input Sensitivity**
K. Honda[1], H. Katsurai[2], M. Nada[2], M. Nogawa[2], H. Nosaka[2]
[1]NTT Corporation, Atsugi-shi, Japan, [2]NTT Corporation, Atsugi-shi, Japan

11:20 a.m.
O.3 **Highly-Integrated Quad-Channel Transimpedance Amplifier for Next Generation Coherent Optical Receiver**
R. Pandey[1], G. Takahashi[2], S. Bhagavatheeswaran[1], E. Tangen[1], M. Heins[1], J. Muellrich[3]
[1]Qorvo, Richardson, United States, [2]Qorvo, San Jose, United States, [3]Micram, Bochum, Germany

11:40 a.m.
O.4 **Silicon Electronics-Photonics Integrated Circuits for Datacenters (Invited)**
S. Shekhar, L. Chrostowski , S. Mirabbasi , S. Nayak, M. W AlTaha, A. Naguib, A. S. Ramani, H. Jayatilleka
University of British Columbia, Vancouver, Canada

12:00 p.m.
End of Session O

12:00 p.m. – 1:30 p.m.
Break for Lunch

PANEL SESSION 3: Reconfigurable RF Systems, Fact or Fiction?

12:00 p.m. – 1:30 p.m.
Phoenix North – Doubletree by Hilton Hotel Austin

Moderators: Tony Quach, *Air Force Research Laboratory*
Nabil El-Hinnawy, *Northrop Grumman*
Taylor Barton, *CU Boulder*

Growing demand for DoD and commercial wireless technologies has created numerous challenges for RF component and system designers. Future systems require operation from VHF to millimeter-wave to maintain legacy systems and expansion for increased data capacity and data rate. However, the expansion in frequency of operation, bandwidth and modulation complexity requires additional RF components and sub-systems that could dramatically increase system cost, size, weight, and power (CSWAP). A potential solution is implementing tunable RF components to enable reconfigurable RF systems capable of frequency agility, power scaling, and waveform diversity. This panel will discuss design techniques and challenges for reconfigurable RF components and systems. Questions to address are: Is reconfiguration RF systems necessary for multi-mode, multi-standard modules? Does increasing system flexibility compromise performance and to what extent? Can a single chip be capable of frequency agility (UHF to mm-wave)? How does an RF system perform concurrent transmit and receive function without interference?

Panel Members:

Gregory Flewelling	BAE Systems
Robert Howell	Northrop Grumman Electronic Systems
Harish Krishnaswamy	Columbia University
Jeyanandh Paramesh	Carnegie Mellon University
Bodhisatwa Sadhu	IBM T.J. Watson Research Center
Russell Wyse	Rockwell Collins

1:30 p.m.
End of Panel Session 3

SESSION P: Low Noise Amplifiers

1:30 p.m. – 3:00 p.m.
Phoenix North - Doubletree by Hilton, Austin

Chairpersons: Don Kimball, *MaXentric*
Shuoqi Chen, *Qorvo*

1:30 p.m.
P.1 **Wideband W-Band GaN LNA MMIC with State-of-the-Art Noise Figure (Invited)**
S. Lardizabal[1], K. C. Hwang[1], J. Kotce[1], A. Brown[1], A. Fung[2],
[1]*Raytheon Company, Andover, MA, United States,* [2]*Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, United States*

2:00 p.m.
P.2 **Low Power Ultra-Wide Band LNA based on Active Impedance Matching Technique for UWB Wireless Communication**
Mantas Sakalas, P. Sakalas, F. Ellinger
Technische Universität, Dresden, Germany

2:20 p.m.
P.3 **Broadband (100MHz -1GHz), High Power Active Circulator Architecture**
J. Kang, H. Sharifi, E. Prophet
HRL, Malibu, United States

2:40 p.m.
P.4 **X-band Robust Current-Shared GaN Low Noise Amplifier for Receiver Applications**
B. Kim, W. Gao
Qorvo, Richardson, United States

3:00 p.m.
End of Session P

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION Q: Next Generation Device Technologies

1:30 p.m. – 3:10 p.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Noriyuki Watanabe, *NTT AT*
Akio Wakejima, *Nagoya Institute of Technology*

1:30 p.m.
Q.1 **Research and Development of InP, GaN and InSb-based HEMTs and MMICs for Terahertz-wave Wireless Communications (Invited)**
I. Watanabe[1], Y. Yamashita[1], A. Endoh[1,3], S. Hara[1], A. Kasamatsu[1], I. Hosako[1],H. Hamada[2], T. Kosugi[2], M. Yaita[2], A. E. Moutaouakil[2], H. Matsuzaki[2], O. Kagami[2], T. Takahashi[3], Y. Kawano[3], Y. Nakasha[3], N. Hara[3], D. Tsuji[4], K. Isono[4], S. Fujikawa[4], and H. I. Fujishiro[4], [1]*National Institute of Information and Communications Technology Tokyo, Japan,* [2]*NTT Device Technology Labs, Kanagawa, Japan,* [3]*Fujitsu Laboratories Ltd., Kanagawa, Japan,* [4]*Tokyo University of Science, Tokyo, Japan*

2:00 p.m.
Q.2 **Recent Progress of Diamond Devices for RF Applications (Invited)**
M. Kasu, *Saga University, Saga, Japan*.

2:30 p.m.
Q.3 **H-Terminated Diamond MISFET with V_2O_5 as Insulator**
S. Colangeli[1], C. Verona[1], W. Ciccognani[1], M. Marinelli[1], G. Rinati[1], E. Limiti[1], M. Benetti[2], D. Cannata[2], F. Di Pietrantonio[2], [1]*Universita di Roma Tor Vergata, Rome, Italy,* , [2]*CNR, Rome Italy*

2:50 p.m.
Q.4 **High Performance SLCFETs for Switched Filter Applications**
J. Parke, R. Freitag, M. Torpey, R. Howell, E. Stewart, M. Snook, I. Wathuthanthri, S. Gupta, B. Nechay, M. King, P. Borodulin, K. Renaldo, H. Henry, *Northrop Grumman Mission Systems, Baltimore, United States*

3:10 p.m
End of Session Q

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION R: Late-Breaking News Papers II

3:30 p.m. – 5:10 p.m.
Phoenix North – Doubletree by Hilton, Austin

Chairpersons: Thé Linh Nguyen, *Finisar Corporation*
Craig Steinbeiser, *Qorvo*

3:30 p.m.
R.1 **A Wideband 341-386 GHz Transmitter in SiGe BiCMOS Technology**
J. Al-Eryani[1,2], H. Knapp[2], J. Wursthorn[2,1], K. Aufinger[2], M. Furqan[3], F. Ahmed[3], H. Li[2], S. Majied[2], L. Maurer[1], [1]Universitaet der Bundeswehr Muenchen, Neubiberg, Germany, [2]Infineon Technologies AG, Neubiberg, Germany, [3]Johannes Kepler University, Linz, Austria

3:50 p.m.
R.2 **A 10-Gb/s, 100-GHz RF Power-DAC Transmitter with On-Die I/Q Driven Antenna Elements and Free-Space Constellation Formation**
S. Shopov[1], O. D. Gurbuz[2], G. M. Rebeiz[2], S. P. Voinigescu[1], *[1]University of Toronto, Toronto, Canada, [2]University of California at San Diego, La Jolla, United States*

4:10 p.m.
R.3 **A High Efficiency, Ka-Band Pulsed Gallium Nitride Power Amplifier for Radar Applications**
P. Blount[1], S. Huettner[2], B. Cannon[2], *[1]Custom MMIC, Chelmsford, United States, [2]Nuvotronics, Durham, United States*

4:30 p.m.
R.4 **A High-Dynamic-Range W-band Frequency-Conversion IC for Microwave Dual-Conversion Receivers**
S. Kim[1], R. Maurer[1], M. Urteaga[2], M. J. Rodwell[1], *[1]University of California, Santa Barbara, Santa Barbara, United States, [2]Teledyne Scientific & Imaging, Thousand, United States*

4:50 p.m.
R.5 **High-Linearity W-band Amplifiers in 130 nm InP HBT Technology**
R. Maurer[1], S. Kim[1], M. Urteaga[2], M. J. Rodwell[1], *[1]UCSB, Santa Barbara, United States, [2]Teledyne Scientific and Imaging, Thousand Oaks, United States*

5:10 p.m.
End of Session R

SESSION S: Late-Breaking News Papers III

3:30 p.m. – 5:00 p.m.
Austin – Doubletree by Hilton, Austin

Chairpersons: Chip Moyer, *HRL Laboratories*
Jim Carroll, *NI-AWR*

3:30 p.m.
S.1 **High Power Monolithic pHemt GaAs Limiter for T/R Module**
B. L. Pham[1], D. P. Nguyen[2], A. Pham[2], P. D. Le[3], *[1]Vimmics Co. Ltd., Da Nang, Viet Nam, [2]University of California Davis, Davis, United States, [3]Le Quy Don Technical University, Hanoi, Viet Nam*

3:50 p.m.
S.2 **A 250 nm GaN N-path Filter IC with +27 dBm Blocker Tolerance**
C. M. Thomas[1,2], T. Quach[3], I. Telliez[1], T. Nakatani[1], D. Kimball[1], L. E. Larson[4], *[1]MaXentric Technologies LLC, La Jolla, United States, [2]University of California San Diego, La Jolla, United States, [3]Air Force Research Laboratory, Wright-Patterson AFB, United States, [4]Brown University, Providence, United States*

4:10 p.m.
S.3 **A Novel 0.1-44 GHz Linear Common-Drain-Cascode 0.15um GaN Distributed Amplifier Architecture with improved IP3-BW**
K. W. Kobayashi, D. Denninghoff, D. Miller, Qorvo, Torrance, United States

4:30 p.m.
S.4 **Compact Phase Accurate Low Loss S-Band 6-Bit Phase Shifter in a 5x5 mm2 Plastic Over Molded Package**
D. Allen, T. Nguyen, Qorvo, Richardson, United States

4:50 p.m.
End of Session S

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SYMPOSIUM CHECKLIST

☐ HOTEL RESERVATIONS

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http://doubletree.hilton.com/en/dt/groups/personalized/A/AUSLNDT-CSI-20161021/index.jhtml?WT.mc_id=PO G

☐ SYMPOSIUM REGISTRATION

Click on the "Online Registration" link on the www.csics.org conference website or go directly to:

http://www.cvent.com/events/2016-ieee-compound-semiconductor-integrated-circuit-symposium-csics-/event-summary-184c0fe480324caa969ef5077746f024.aspx

Advance registration deadline: September 23rd.

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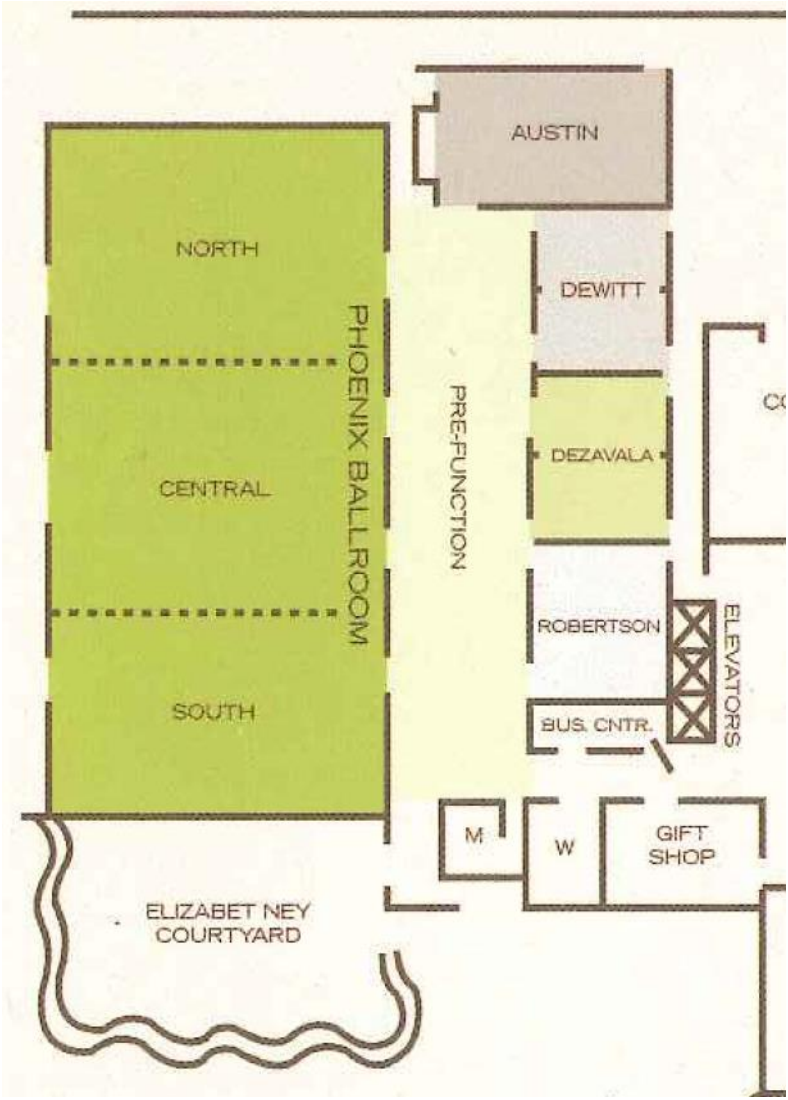

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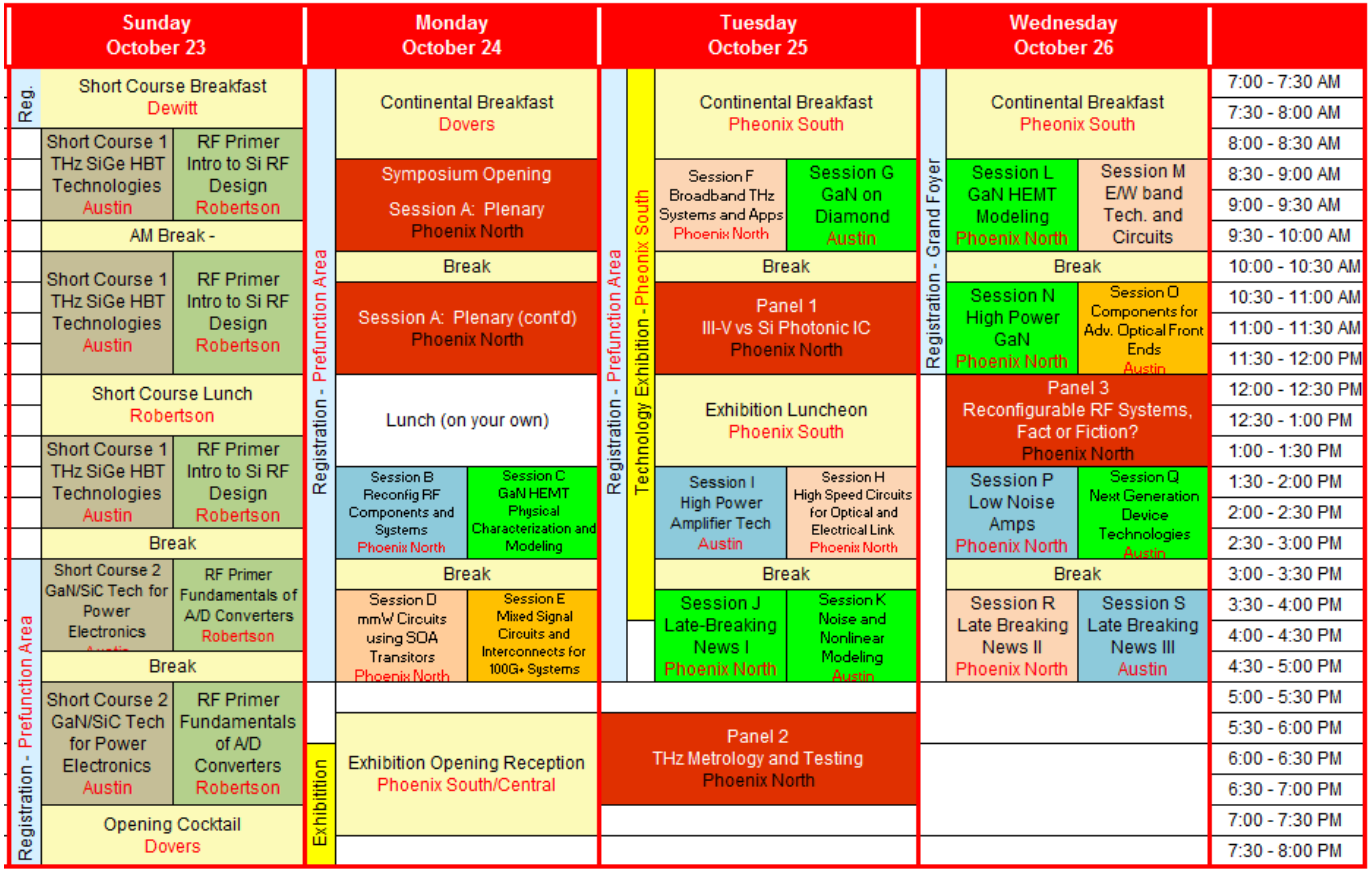

Please note that the times are approximate. Please refer to the detailed schedule on pp. 2 and 3.

CSICS Week – Schedule Overview

NOTES