34th IEEE COMPOUND SEMICONDUCTOR IC (CSIC) SYMPOSIUM

Program

Presenting:

CSICS:Riding the New Wave

Oct 14th – Oct 17th, 2012
Hyatt Regency La Jolla at Aventine

La Jolla, California, USA

CO- SPONSORED BY
The IEEE Electron Devices Society,
The IEEE Solid-State Circuits Society, and
The IEEE Microwave Theory and Techniques Society.

SYMPOSIUM

Saturday, October 13th, 2012
REGISTRATION (Short Courses & Primer Course Only)

Sunday, October 14th, 2012
REGISTRATION (Short Courses & Primer Course Only)
Short Course Continental Breakfast
SHORT COURSE 1: The Future of Compound Semiconductor Devices
Short Course Lunch
REGISTRATION for Symposium
SHORT COURSE 2: Thermal Management
PRIMER COURSE: Basics of Compound Semiconductor ICs
CSIC Symposium Opening Cocktail

Monday, October 15th, 2012
REGISTRATION
Continental Breakfast
SYMPOSIUM OPENING
SESSION A: Plenary Session
SESSION B: GaN Power Amplifiers
SESSION C: Heterogeneous Integration
SESSION D: mm-Wave Transceivers and Building Blocks
SESSION E: High Frequency Technology
Exhibition Opening Reception
Technology Exhibition

Tuesday, October 16th, 2012
REGISTRATION
Technology Exhibition
Continental Breakfast
SESSION F: HEMT/FET Modeling
SESSION G: Advanced Electro-Optical Components
PANEL SESSION 1: Circuit Design with FEM EM Simulators
Does an IC designer really need arbitrary 3D EM Analysis?
Exhibition Lunch
SESSION H: Thermal Management
SESSION I: RF CMOS Circuits
PANEL SESSION 2: Is Diamond the Answer for High Power Density GaN?

Wednesday, October 17th, 2012
REGISTRATION
Continental Breakfast
SESSION J: Design Techniques for High Efficiency Power Amplifiers
SESSION K: mm-Wave Amplifiers
SESSION L: High Power Technologies
SESSION M: Receiver Circuits
SESSION N: Power Amplifier Modules
SESSION O: High Speed Mixed Signal Circuits
SESSION P: Breaking News Papers

Close of Symposium

AT A GLANCE

Saturday, October 13th, 2012

4:00 p.m. – 6:00 p.m.	Grand Foyer

Sunday, October 14th, 2012

7:00 a.m. – 8:00 a.m.	Grand Foyer
7:00 a.m. – 8:00 a.m.	**Mykonos AB**
7:30 a.m. – 2:30 p.m.	Delphi AB
12:15 p.m. – 1:45 p.m.	**Mykonos AB**
3:00 p.m. – 8:00 p.m.	Grand Foyer
4:00 p.m. – 7:00 p.m.	Delphi AB
3:00 p.m. – 6:00 p.m.	Athenia AB
7:00 p.m. – 8:30 p.m.	**Grand Foyer**

Monday, October 15th, 2012

7:00 a.m. – 5:00 p.m.	Grand Foyer
7:00 a.m. – 8:30 a.m.	**Grand Foyer**
8:30 a.m. – 9:00 a.m.	Aventine ABC
9:00 a.m. – 11:45 p.m.	Aventine ABC
1:30 p.m. – 2:30 p.m.	Aventine ABC
1:30 p.m. – 3:10 p.m.	Aventine DE
3:30 p.m. – 5:50 p.m.	Aventine ABC
3:30 p.m. – 5:50 p.m.	Aventine DE
6:00 p.m. – 7:30 p.m.	**Pavilion**
6:00 p.m. – 8:00 p.m.	**Pavilion**

Tuesday, October 16th, 2012

7:00 a.m. – 5:00 p.m.	Grand Foyer
7:00 a.m. – 4:00 p.m.	Pavilion
7:00 a.m. – 8:30 a.m.	**Pavilion**
8:30 a.m. – 10:00 a.m.	Aventine ABC
8:30 a.m. – 10:10 a.m.	Aventine DE
10:30 a.m. – 12:00 p.m.	Aventine ABC
12:00 p.m. – 1:30 p.m.	**Pavilion**
1:30 p.m. – 3:10 p.m.	Aventine ABC
1:30 p.m. – 3:00 p.m.	Aventine DE
3:30 p.m. – 5:00 p.m.	Aventine ABC

Wednesday, October 17th, 2012

7:00 a.m. – 12:00 p.m.	Grand Foyer
7:00 a.m. – 8:30 a.m.	**Grand Foyer**
8:30 a.m. – 9:40 a.m.	Aventine ABC
8:30 a.m. – 10:10 a.m.	Aventine DE
10:30 a.m. – 11:50 a.m.	Aventine ABC
10:30 a.m. – 11:50 a.m.	Aventine DE
1:30 p.m. – 2:50 p.m.	Aventine ABC
1:30 p.m. – 2:40 p.m.	Aventine DE
3:30 p.m. – 5:10 p.m.	Aventine ABC

5:10 p.m.

Visit us at: http://www.csics.org

CHAIR'S MESSAGE

On behalf of the Symposium organizing committee, the IEEE Electron Devices Society, the Microwave Theory and Techniques Society, and the Solid-State Circuits Society, we invite you to be a part of the 2012 IEEE Compound Semiconductor IC Symposium (CSICS). This will be the 34th year that the IEEE CSICS (originally GaAs IC Symposium) has been held. We have chosen to locate this year's Symposium in beautiful La Jolla, California.

From its beginning in 1978 as the GaAs IC symposium, the IEEE Compound Semiconductor IC Symposium (CSICS) has evolved to become the preeminent international forum for developments in compound semiconductor integrated circuits and devices, embracing GaAs, InP, GaN, SiGe, and more recently CMOS and 2-D crystal device technology. Who would have thought in 1978, or even as recently as 2005, that CMOS would join the compound semiconductor device family, and that III-V and Ge channels would become serious contenders for the 14 nm node?

This year, coverage includes all aspects of the technology, from materials and device fabrication and modeling to IC design and testing, high volume manufacturing, and system applications. Additionally, the latest results in high-speed digital, analog, microwave, millimeter wave, THz, mixed-signal, and optoelectronic integrated circuits will be presented.

There are several social events that allow our attendees to interact in a relaxed setting. These include the Sunday Evening Opening Cocktail Hour, the Monday evening Exhibition Opening Reception and the Technology Exhibition Luncheon on Tuesday. We also offer daily breakfast and AM/PM coffee breaks Monday through Wednesday.

The IEEE CSICS will offer two short courses this year. The first will be "The Future of Compound Semiconductor Devices" covering III-V and Ge channel MOSFETs, GaN HEMTs and Graphene transistors. The second will be "Thermal Management", covering a critical but rarely discussed topic in IC and device design. In addition, we offer our "Primer Course" on the basics of semiconductor ICs which is an excellent tutorial presented within the context of our Symposium technical program. All three courses will be offered on Sunday Oct. 14th, 2012.

Please join us "Riding the New Wave" of Compound Semiconductor Devices and IC's!

Sorin Voinigescu
2012 IEEE CSICS Chair

CORPORATE BENEFACTORS

This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support of the Symposium by making contributions towards the cost of some of our social events.

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. To discuss any of the benefactor opportunities in more depth, please contact:

Sorin Voinigescu
Tel: +1-416-946-8664
E-mail: sorinv@eecg.toronto.edu

As of this printing, the Corporate Benefactors for the 2012 Compound Semiconductor IC Symposium are as follows.

Gold Level Benefactor

RF Micro Devices, Inc.

Silver Level Benefactors

Agilent Technologies

Maury Microwave Corporation

AWR Corporation

TriQuint Semiconductor

OMMIC

The Symposium Web Site www.csics.org has become a critical tool for the dissemination of information to prospective attendees, committee members and sponsors of the Symposium. Every year, the web site must be updated and maintained to effectively serve this purpose. We would like to acknowledge the following benefactor for providing the Symposium web site support for the 2012 CSIC Symposium:

This year we are pleased to welcome

as our media partner.

Comments regarding the web site or any publicity materials should be directed to the Publicity Chair, Jim Carroll (jim.carroll@awrcorp.com). Links to our corporate benefactors appear on our symposium website.

GENERAL INFORMATION

IEEE 34th CSIC Symposium
Oct 14th - Oct 17th, 2012
Hyatt Regency La Jolla at Aventine
La Jolla, California, USA

REGISTRATION

	Advance (Received by Sept. 24th)	Regular (After Sept. 24th or on site)
Symposium Registration		
IEEE Member	$645	$695
Non-IEEE	$695	$795
IEEE Life-Member	$325	$325
Student	$325	$325
Special One-day IEEE Member[1]	$300	$350
Special One Day Non-IEEE[1]	$355	$415
Short/Primer Course		
Short Course 1+2	$400	$400
Short Course 1+2 Student	$200	$200
Primer Course	$250	$250
Primer Course Student	$150	$150
Additional Items		
Guest Opening Cocktail Reception Ticket	$40	$40
Guest Exhibition Opening Reception Ticket	$80	$80
Adtl. Digest USB	$100	$100
Adtl. Short Course USB	$100	$100
Adtl. Short Course Notes USB	$50	$50
Adtl. Exhibitor Registration	$325	$395

All fees are denominated in US$

Full Registration Includes: USB Digest, Opening Cocktail, all technical sessions, panels, exhibits, Exhibition Opening Reception, Exhibition Lunch, and all coffe breaks.

Short Course Registration Includes: Short Course Notes on USB, continental breakfast and Short Course Lunch

[1]Special One-day Registration Includes: USB only (no social functions)

Primer Course Registration includes: Primer Course Notes on USB Only

For **ADVANCE REGISTRATION,** click on the Symposium Registration link on the Symposium website (www.csics.org). You may register either through the website or complete the enclosed Advance Registration Form with your remittance of the appropriate fee (check or credit card) **by September 24th, 2012**. Prices will increase after the September 24th deadline.

Mail or Fax Completed Advance Registration Form to:

IEEE/MCM: Lukrecija Lelong, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-732-562-5441

Toll Free (US or Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csicsreg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency or traveler's checks. Checks must be made payable to "IEEE/2012 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

When you register for the Conference, the contact information you provide (including your name, address, phone, and email address) may be shared with CSICS and vendor exhibitors.

We urge you to pre-register to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

Registration Center:

The Symposium Registration Center is located in the Grand Foyer on Saturday through Wednesday. The operating hours will be as follows:

Short & Primer Course Registration only

Saturday, October 13th	4:00 p.m. – 6:00 p.m.
Sunday, October 14th	7:00 a.m. – 8:30 a.m.
Sunday, October 14th	3:00 p.m. – 4:00 p.m. (Primer)

Symposium Registration

Saturday, October 13th	4:00 p.m. – 6:00 p.m.
Sunday, October 14th	3:00 p.m. – 8:00 p.m.
Monday, October 15th	7:00 a.m. – 5:00 p.m.
Tuesday, October 16th	7:00 a.m. – 5:00 p.m.
Wednesday, October 17th	7:00 a.m. – 12:00 p.m.

Refund Policy:

All requests for refund/cancellation must be received in writing by September 25th, 2012. No refunds can be provided after this date. Cancellations will incur a US$50 administration fee. Please submit cancellation requests via email to csicsreg@ieee.org

Mail or Fax Completed Advance Registration Form to:
IEEE/MCM: Lukrecija Lelong, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-732-562-5441
Toll Free (US or Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csicsreg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency or traveler's checks. Checks must be made payable to "IEEE/2012 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

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ACCOMMODATIONS

Hotel Reservations:

A block of rooms has been reserved at special discounted rates for Symposium participants at our headquarters hotel, Hyatt Regency La Jolla at Aventine. Enjoy a seaside destination with the charm of a European village and the panache of Southern California. Located in the city known as "The Jewel of the Pacific", the hotel offers incomparable beaches, shopping, dining, galleries and attractions. Visit Stephen Birch Aquarium & Museum, spend a day kayaking, take a Baja Lobster or Wine tour, see live theater or shop San Diego's trendy boutiques. Accommodations were recently refreshed and now include 42" flat screen TVs, an iHome stereo with iPod® docking station, in-room safe, complimentary daily newspaper, and Portico bath products. High-speed wireless Internet is available at nominal daily charge. Wheelchair accessible rooms are available.

Hotel Address and Phone Numbers:

Hyatt Regency La Jolla at Aventine
3777 La Jolla Village Drive,
San Diego, California, USA 92122
Tel: +1 858 552 1234
Fax: +1 858 552 6066
Web Site: http://www.hyattregencylajolla.com

While there are alternatives, we would like to remind attendees to please support the Symposium and fully enjoy all the activities on offer by staying at the official headquarters hotel. The Symposium relies on attendees staying at the conference Hotel to reduce the costs charged for the use of meeting rooms. Room reservations should be made as soon as possible, as there are a limited number available at the symposium rate. To qualify for the discounted rate reservations must be made by 5:00pm Pacific time, September, 12 2012. Rooms are available at the special Symposium group rate of US$165.00 per night. These rates do not include room taxes, which are %12.6.

To make a reservation, you can follow the link on the symposium website or contact the hotel direct at +1-858-552-1234 and ask for Reservations. Be certain to request the Special Group Rate for the IEEE CSIC Symposium or on-line at

https://resweb.passkey.com/Resweb.do?mode=welcome_ei_new&eventID=7392428.

Rooms will be subject to availability and possibly be charged at higher rates. Check-in time is 3 p.m. or later; check-out time is 12 noon. If necessary, you may cancel your reservation 24 hours prior to arrival to avoid a one (1) night plus tax penalty charge.

TRANSPORTATION

Travel Arrangements:
Special Airfares:

Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc by calling between the hours of 8:00 a.m. and 5:30 p.m. EST Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 717 556 1100. Or, you may visit their on-line travel service web site at http://www.ieee.org/travel. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Or you can e-mail your request to ieee@worldtravelinc.com.

IEEE corporate car rental discounts are also available to all attendees of the symposium. Discount codes below entitle attendees to receive special rates that have also been negotiated with Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.

Airport Transportation:

The San Diego International Airport/Lindberg Field (SAN) is about 10 miles from the Hyatt Regency La Jolla at Aventine. The airport accommodates domestic and international travel.

Airport Transfer:

Transfer to and from the airport can be made by means of shuttle or taxi. Express Shuttle or Cloud 9 Shuttle: Cost: approx US$15.00 one way per person (subject to change) with pick up outside of baggage claim area.
Taxi: approx US$35-US$45 one way with pick up outside of baggage claim area.

Driving Directions:

From San Diego Int'l Airport (10 miles)**:** Turn left on Harbor Drive, then left again on Laurel. Follow signs to I-5 North. Exit at La Jolla Village Drive and turn right. Turn right again at Lebon. Turn right on University Center Lane into the hotel.

ADDITIONAL INFORMATION

Distribution of Relevant Information:

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to be indiscriminately proliferated in the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition.

Photography:

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. No flash photography will be used. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE. Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.

Non Discrimination Policy

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws. For more information on the IEEE policy visit, http://www.ieee.org/about/corporate/governance/p9-26.html?WT.mc_id=hpf_pol

Breakfast and Lunch Locations:

Breakfasts:

The location of breakfasts will be as follows:

Short Course Registrants (only) –
Sunday, October 14th Mykonos AB

Symposium Registrants –
Monday, October 15th: Grand Foyer
Tuesday, October 16th: Pavilion
Wednesday, October 17th: Grand Foyer

Lunches:

The location of lunches will be as follows:

Short Course Registrants (only) –
Sunday, October 14th: Mykonos AB

Exhibition Luncheon –
Tuesday, October 16th: Pavilion

Coffee Breaks:

The location of coffee breaks will be as follows:

Short Course and Primer Course registrants (only) –
Sunday, October 14th — second floor conference level

Symposium Registrants –
Monday, October 15th: Grand Foyer
Tuesday, October 16th: Pavilion
Wednesday, October 17th: Grand Foyer

Symposium Social Events:

SYMPOSIUM Opening Cocktail

We welcome you to San Diego on Sunday evening, October 14th from 7:00 p.m. to 8:30 p.m. in the Grand Foyer of the Hyatt Regency La Jolla at Aventine. Come and meet up with your old friends and make new acquaintances over cheese and wine, beer or soft drinks. One free admission is included with your registration including two drink tickets, and extra reception tickets may be purchased at registration for $40.

EXHIBITION OPENING RECEPTION

The exhibition opening reception will be held on Monday evening, October 15th from 6:00 p.m. to 7:30 p.m. in the Pavilion of the Hyatt Regency La Jolla at Aventine. Come along; visit with the exhibitors over light hors d'oeuvres and wine, beer, or soft drinks. One free admission is included with your registration, and extra reception tickets may be purchased at registration for $80.

EXHIBITION LUNCHEON

On Tuesday, October 17th at noon the Exhibition Luncheon will be hosted in the Pavilion. The lunch is free to all Symposium participants, so come along, visit with the exhibitors, ask questions, make deals and find out what is going on in our industry.

San Diego Attractions:

So much more than a pretty beach, San Diego is a laid-back spectacle of history, culture and wildlife. An estimated 1.36 million people call it their home, which stretches from the northern coasts of La Jolla and Pacific Beach, down to Mission Valley, Old Town and bustling Downtown San Diego. San Diego's roots trace back to the 1880s, and much of that historic character is retained in Downtown San Diego's Gaslamp District, not far from Manchester Grand Hyatt. The corridor is toasting to urban revival's finest hour, thanks to covert lounges and wine bars, trendy fashion boutiques and some of the finest craft beer selections on the planet (San Diegans love their IPAs). Equally legendary is the centrally located Balboa Park, home to 15 museums and the world-famous San Diego Zoo—one of three major animal attractions in the area. The 1,200-acre park is one of the oldest urban parks in the country, second only to New York's Central Park. Here, you find nearly all of the city's art galleries and theaters—including the famous Old Globe.

SYMPOSIUM HIGHLIGHTS

Technical Program:

The technical program for the 2012 IEEE CSIC Symposium consists of 63 technical papers, 2 panel sessions, an industry exhibit, and 2 short courses "The Future of Semiconductor Devices and Integrated Circuits" and "Advanced Thermal Management for Wide Bandgap (WBG) Devices and Circuits." We will also be offering our annual introductory level class "Basics of Compound Semiconductor ICs" (Primer Course).

This year we have invited 19 papers on a wide range of important topics encompassing advanced device engineering to circuit application using compound and other related semiconductor technologies.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. This year there is considerable interest in GaN devices, heterogeneous integration, semiconductor processes for >100 GHz applications, and thermal management of high power devices. As always there is a tremendous amount of activity in wireless communications and military electronics.

Late-Breaking News Papers:

We have solicited papers containing late-breaking news for the Symposium Program. The times and locations of these presentations will be posted on the Symposium website.

Technical Digest:

Extra USB Technical Digests can be purchased by Symposium registrants through Advance Registration. A limited number of Digests USBs may also be available for sale at the Registration Desk. The cost of the USB ordered through Advance Registration or purchased on-site is $100.

Outstanding Paper Award:

The 2012 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the Session Chairpersons. The award winner will be publicly announced shortly after this year's Symposium with the award formally presented during the next year's CSIC Symposium.

Short Course 1: "The Future of Semiconductor Devices and Integrated Circuits"

Short Course Description

Semiconductor device technology is on the verge of a new era. There are concerns that over the next decade Moore's Law might come to an end. Indeed, planar scaling of conventional Si/SiO_2 MOSFETs has already been pushed beyond its natural limit by the introduction of strained silicon channels in 90 nm, high-K dielectrics and metal gates in 45 nm, and finally 3D tri-gates in 22 nm. What will it take to get below 14 nm and subsequently 7 nm? At the same time, Wide Bandgap (WBG) devices have created whole new application areas by leveraging their unique high power/high frequency capabilities. What are GaN's prospects for realizing its full potential for THz power generation and ultimately reaching the levels of manufacturability of conventional semiconductors like Si or GaAs? Will a new generation of 2D materials systems with intriguing properties address the difficulties of conventional semiconductors? Will they create altogether new and unexpected opportunities? This course covers three different semiconductor device technologies, each of which introduces new materials and challenges the current limits of performance.

Short Course 2: "Advanced Thermal Management for Wide Bandgap (WBG) Devices and Circuits"

Short Course Description

The promised performance of wide bandgap (WBG) electronic devices results in much higher power dissipation and localized heat generation at the contacts and in the channel than can be accommodated by the current thermal management state-of-the-art (SoA). As a consequence, use of conventional cooling techniques imposes a ceiling on WBG device performance and reliability. Overcoming such barriers requires thermal engineering, at the micro- and nano-scale, which can provide significant reductions in the near-junction temperature rise and component thermal resistance.

This course will provide the tools and insights required to achieve improved thermal management of WBG devices. It will start with a brief review of WBG transistor morphology and heat generation and identify the primary thermal–electrical–fabrication trade-offs in MMIC design. Next, participants will receive an overview of heat transfer principles and the SoA in thermal packaging, including on-chip cooling. Attention will then turn to the analytical and numerical thermal modeling of wide bandgap transistors and MMICs and explore the primary trends and parametric sensitivities of channel temperature to device geometry, material properties, and convective as well as thermal boundary resistances. The course will conclude with a brief look at current and planned thermal packaging research and an open discussion on the content and the primary "take-aways" from this course.

This Thermal Management short course is aimed at device engineers, MMIC designers, system developers, and researchers alike. Participants will gain insight into the underlying thermal phenomena which can limit or enable the performance of compound semiconductor devices. The course will impart a functional knowledge of heat transfer principles and governing relations for estimating device temperatures. Following the presentation, discussion time will be

provided. A copy of the viewgraphs will be distributed to each course registrant.

The instructors for this course, Dr. Avram Bar-Cohen and Dr. Jonathan Felbinger, are at the forefront of thermal packaging technology development at the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA/MTO).

Direct questions to:

Douglas S. McPherson, Short Courses Coordinator
Ciena Corporation
(613) 670-3371
dmcphers@ciena.com

Panel Sessions:

This year we have two exciting Panel Sessions on Tuesday October 16th.. These are intended to be timely, thought-provoking, educational, and hopefully controversial. The two panel topics are as follows:

PANEL SESSION 1:
Circuit Design with FEM EM Simulators - Does an IC designer Really Need Arbitrary 3D EM Analysis?
Tuesday, October 16th, 10:30-12:00 noon

PANEL SESSION 2:
Is Diamond the Answer for High Power Density GaN?
Tuesday, October 16th, 3:30-5:00 p.m.

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to day and time).

Technology Exhibition:

The 2012 IEEE CSICS Technology Exhibition will be held on Monday evening October 15th and Tuesday the 16th in the Pavilion and is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, as well as the latest information on modeling and design simulation tools. This year's exhibitors include:

Accel-RF Corporation
Agilent Technologies
Anritsu Company
ANSYS
AWR Corporation
Axiom Test Equipment
Compugraphics
CST of America
Lehighton Electronics
Maury Microwave
Nuhertz Technologies
Presidio Components
Quik-Pac
Sonnet Software
StratEdge Corporation

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 6:00 p.m. and 8:00 p.m. on Monday, October 15th, and between 7:00 a.m. and 4:00 p.m. on Tuesday, October 16th. The Exhibition will also host the Exhibition Opening Reception from 6:00 p.m. until 7:30 p.m. on Monday evening and the Exhibition Luncheon from 12:00 noon to 1:30 p.m. on Tuesday. The Exhibition Opening Reception, the Exhibition Luncheon, and the Tuesday coffee breaks will be held in the exhibition area in the Pavilion.
For participating in the Exhibition, please contact Harry Kuemmerle (VIP Meetings & Conventions), harry.k@vipmeetings.com Tel: (310) 459-4691; FAX: (310) 459-0605. Please visit the Symposium website at http://www.csics.org/ for additional information.

Short Courses

Sunday, October 14th, 2012
Hyatt Regency La Jolla at Aventine

Course Coordinator: **Douglas S. McPherson**
Ciena Corp.
613-670-3371
dmcphers@ciena.com

"The Future of Semiconductor Devices and Integrated Circuits"

This course presents in detail three different emerging semiconductor device technologies, each of which challenges the current limits of performance in their own respective way. The course opens with a lecture on GaN HEMT device technology. While relatively mature compared to other emerging technologies, GaN HEMTs are well known for demonstrating a ten-fold improvement in power density compared to GaAs PHEMTs. With recent improvements in material quality, gate and epitaxial-layer design, GaN HEMTs now have the potential for generating significant power in the lower portion of the "terahertz gap," that is frequencies above 100 GHz. From high power applications, the course turns to high-density, ultra-low power digital CMOS, where traditional scaling is reaching its limit. The second lecture focuses on III-V CMOS, a technology that exploits the superior transport properties of III-V semiconductors to overcome the mounting difficulties that Si is encountering in continuing Moore's Law. The final lecture is on epitaxial-graphene field-effect transistors (GFETs) and their application to RF circuit design. Like III-V CMOS technology, graphene based FETs introduce a new channel material with extraordinary carrier mobility, as well as large on-state current density. GFETs are fabricated with HfO_2 gate dielectric and metal gate, similar to advanced-node MOSFETs. Their unique 2D channel properties make them ideal for use in RF mixers, RF detectors, radiometers, and frequency multipliers. Indeed, measured RF results in the millimeter-wave frequency ranges show how GFETs are becoming a disruptive technology. Although significant challenges remain to be overcome, emerging GFETs also have the potential to be integrated alongside standard Si MOSFETs, thus enabling a new generation of high performance RF SoCs.

Topics Covered and Instructors:

1) GaN Devices for Terahertz Power – Robert J. Trew, NSF, United States
2) Nanometer-Scale III-V CMOS – Jesús A. del Alamo, MIT, United States
3) Graphene Transistors for RF Applications – Jeong-Sun Moon, HRL, United States

"Advanced Thermal Management for Wide Bandgap (WBG) Devices and Circuits"

This Thermal Management short course is aimed at device engineers, MMIC designers, system developers, and researchers alike. Participants will gain insight into the underlying thermal phenomena which can limit or enable the performance of compound semiconductor devices. The course will impart a functional knowledge of heat transfer principles and governing relations for estimating device temperatures. Following the presentation, discussion time will be provided. A copy of the viewgraphs will be distributed to each course registrant.

The instructors for this course, Dr. Avram Bar-Cohen and Dr. Jonathan Felbinger, are at the forefront of thermal packaging technology development at the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA/MTO).

Short Course Outline

1. MMIC Packaging and Trade-Offs
   - 1.1. Morphology of WBG Transistors and MMICs
   - 1.2. Thermal Characteristics of WBG Transistors and MMICs
   - 1.3. Thermal–Electrical–Fabrication Trade-Offs in MMIC Design
2. Thermal Management Technology
   - 2.1 Principles of Heat Transfer
   - 2.2 State-of-the-Art in Thermal Packaging
   - 2.3 On-Chip Cooling
3. Advanced Thermal Management of WBG Devices
   - 3.1 Thermal Modeling of WBG HEMTs and MMIC PAs
   - 3.2 Primary Thermal Trends and Parametric Sensitivities
   - 3.3 Current and Planned Thermal Packaging Research
4. Closure
   - 4.1 Lessons Learned ("Take-Aways")
   - 4.2 Open Discussion with Instructors

Schedule

3:00 p.m. **MMIC Packaging and Trade-Offs**
Jonathan Felbinger, Booz Allen Hamilton

3:45pm **Thermal Management Technology**
Avram Bar-Cohen, DARPA

4:45 p.m. **Coffee Break**

5:15 p.m. **Advanced Thermal Management of WBG Devices**
Jonathan Felbinger, Booz Allen Hamilton
Avram Bar-Cohen, DARPA

6:45 p.m. **Questions and Discussion**

7:00 p.m. **Close of Short Course**

Short Course Instructors

Dr. Avram Bar-Cohen is a Program Manager in the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA), Arlington, VA; he is serving in this capacity while on leave from his position as a Distinguished University Professor at the University of Maryland, where he most recently also served as the Chair of the Mechanical Engineering Department (2001-2010). Dr. Bar-Cohen earned a Ph.D. in Mechanical Engineering from the Massachusetts Institute of Technology and prior to joining Maryland,

Dr. Bar-Cohen directed the University of Minnesota's Center for the Development of Technological Leadership. His publications, lectures, short courses, and research, as well as professional service in ASME and IEEE, have helped to create the scientific foundation for the thermal management of electronic components and systems. Dr. Bar-Cohen was the recipient of the prestigious International Centre for Heat and Mass Transfer's 2008 Luikov Medal, ASME's Heat Transfer Memorial Award (1999), and the IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (2002). He is among a very select number of ASME Honorary Members and is a Fellow of IEEE.

Dr. Jonathan Felbinger is a consultant with Booz Allen Hamilton and has supported DARPA/MTO since March 2012. In 2010 he earned his Ph.D. in Electrical Engineering from Cornell University, supported by the Lester F. Eastman Fellowship, after which he joined the Microwave Electronics Laboratory (MC2-MEL) at Chalmers University of Technology. Dr. Felbinger's research interests include thermal management of semiconductor devices; design, fabrication, and characterization of high-frequency HEMTs and MMICs; and microwave and millimeter-wave electronics. He authored the Best Student Paper at WOCSDICE 2007 and co-authored the Exceptional Outstanding Paper at MIPRO 2010 in addition to several journal articles and a book chapter. He is a member of the IEEE.

Short Course Schedule

The short courses are held on Sunday October 14th in the second floor conference level, rooms Delphi AB and Athenia AB. A continental breakfast is available to all registered Short Course attendees and instructors. The first course "The Future of Semiconductor Devices and Integrated Circuits" will begin at 7:30 am and finish at 2:30 pm. A lunch will be provided as well as morning and afternoon refreshment breaks.

The second short course "Advanced Thermal Management for Wide Bandgap (WBG) Devices and Circuits" will begin at 3:00 pm and finish at 7:00 pm and includes a refreshment break. All participants are invited to join the Symposium Opening Reception at 7:00 pm in the Grand Foyer.

7:00 a.m. **Registration and Breakfast**

Short Course I – The Future of Semiconductor Devices and Integrated Circuits

Dephi AB

7:30 a.m. **Introduction and Overview**

7:45 a.m. **GaN Devices for Terahertz Power**
Robert J. Trew, NSF, United States

9:30 a.m **Coffee Break**

10:00 a.m. **Nanometer-scale III-V CMOS**
Jesús A. del Alamo, MIT, United States

11:45 a.m. **Lunch**

12:45 p.m. **Graphene transistors for RF applications: will it be disruptive?**
Jeong-Sun Moon, HRL, United States

2:30 p.m. **Coffee Break and Q&A**

3:00 p.m. **Close of Short Course**

Short Course II - Advanced Thermal Management for Wide Bandgap (WBG) Devices and Circuits

Dephi AB

3:00 p.m. **MMIC Packaging and Trade-Offs**
Jonathan Felbinger, Booz Allen Hamilton, United States

3:45 p.m. **Thermal Management Technology**
Avram Bar-Cohen, DARPA, United States

4:45 p.m. **Coffee Break**

5:15 p.m. **Advanced Thermal Management of WBG Devices**
Jonathan Felbinger, Booz Allen Hamilton
Avram Bar-Cohen, DARPA, United States

6:45 p.m. **Questions and Discussion**

7:00 p.m. **Close of Short Course**

Who Should Attend

The future of semiconductors course is intended to appeal to both technologists and circuit designers with an interest in nano-scale fabrication and circuit design. Each lecture will cover the merits, principles, and manufacturability challenges of these new technologies and provide comparison with existing and competing technologies. While the emphasis is on device physics, processing, and transistor characterization, the course also includes examples illustrating how these technologies relate to future high-speed analog/digital and RF/mm-wave circuit design. The course is presented by Dr. Robert J. Trew, Prof. Jesús del Alamo, and Dr. Jeong-Sun Moon, all renowned experts in their respective fields.

The thermal management short course is aimed at device engineers, MMIC designers, system developers, and researchers alike. Participants will gain insight into the underlying thermal phenomena which can limit and or enable the performance of compound semiconductor devices. The course will impart a functional knowledge of heat transfer principles and governing relations for estimating device temperatures. The instructors for this course, Dr. Avram Bar-Cohen and Dr. Jonathan Felbinger, are at the forefront of thermal packaging technology development at the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA/MTO).

Our lecturers will cater to a range of interests and experience levels. Each course is designed to strike a balance between a comprehensive overview of the course's main subject and in-depth information on the most pertinent topics.

Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for the Short Courses. A limited number of Short Course registrations will be available on site Sunday October 14th 7:00 am – 8:00 am. The registration fee for Short Course I and II is $400 for professionals and $200 for students. This includes attending the lectures, notes for both Short Courses on a USB stick, a continental breakfast, a lunch and morning/afternoon refreshments during breaks. Additional copies of the Short Course Notes on USB may be purchased for $100 each.

Primer Course

Sunday, October 14th, 2012
Hyatt Regency La Jolla at Aventine
Athenia AB
3:00 p.m. - 6:00 p.m.

"Basics of Compound Semiconductor ICs"

Instructors:

Stephen I. Long
University of California
at Santa Barbara
Santa Barbara, CA

Donald B. Estreich
Sonoma State University
Santa Rosa, CA

Course Coordinator:

Harris P. Moyer
HRL Laboratories, LLC

Course Objective and Description:

The popular primer course "Basics of Compound Semiconductor ICs" is an introductory-level class intended for professionals in the electronic industry with little or no experience in compound semiconductor IC technology. It also provides an excellent review for those with more experience. The course covers: digital and analog/RF/microwave circuits; III/V materials including wide bandgap GaN and SiC; MOS and bipolar devices. The course is tailored to provide background for symposium participants to better understand and appreciate the papers presented, including a glossary of those ever-cryptic acronyms. Throughout the course, comparisons among the compound semiconductor technologies will be presented as well as comparisons with silicon technologies. Also, a number of compound semiconductor integrated circuits will be described along with their intended applications.

Instructors Stephen I. Long and Donald B. Estreich each have over 25 years of experience working with compound semiconductor ICs. A USB flash drive containing the viewgraphs and an extensive bibliography will be distributed to each Primer Course registrant. Ample discussion time will provide an opportunity for participants to have questions answered by the instructors.

Course Agenda:

3:00 p.m. Introduction
3:05 p.m. Compound Semiconductor Materials
3:30 p.m. Device Operation
4:00 p.m. Discussion
4:10 p.m. Analog/RF/Microwave Circuits
4:30 p.m. Coffee Break
4:40 p.m. Analog/RF/Microwave Circuits (continued)
5:00 p.m. RFIC Design Examples
5:40 p.m. Summary and Discussion
6:00 p.m. Close

The advanced registration fee is $250 for professionals and $150 for students and includes the aforementioned USB flash drive. Additional flash drives may be purchased for $50. Space is limited, so ADVANCE REGISTRATION IS HIGHLY RECOMMENDED. For additional information, please contact the Primer Course Coordinator.

Primer Course Coordinator:
Harris Moyer, Primer Course Organizer and Chair
HRL Laboratories, LLC
3011 Malibu Canyon Rd.
Malibu, CA 90265 USA
(310)317-5784 hpmoyer@hrl.com

CSIC Symposium Opening Cocktail Hour

Grand Foyer

7:00 p.m. - 8:30 p.m.

Monday, October 15th, 2012

SYMPOSIUM PROGRAM

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Grand Foyer– Hyatt Regency La Jolla at Aventine
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Grand Foyer

SYMPOSIUM OPENING

8:30 a.m. – 9:00 a.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Opening Remarks
2012 Symposium Chair
Sorin Voinigescu, *University of Toronto*

Technical Program Overview
2012 Technical Program Chair
Francois Colomb, *Raytheon*

SESSION A: PLENARY SESSION

9:00 a.m. – 11:45 a.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Douglas McPherson, *Ciena Corporation*
Harris Moyer, *HRL Laboratories*

9:00 a.m.
A.1 **DARPA's Microscale Power Conversion Program (Invited)**
J. D. Albrecht[1], A. Kane[2], T. Chang[2], *[1]DARPA, Arlington, United States, [2]Booz Allen Hamilton Inc, Arlington, United States*

9:30 a.m.
A.2 **Landing Radar Technology at the Jet Propulsion Laboratory: Mars Science Laboratory and Beyond (Invited)**
B. Pollard, *Jet Propulsion Laboratory, Pasadena, United States*

10:00 a.m. - 10:15 a.m.
Coffee Break

10:15 a.m.
A.3 **Towards Millimeter-Wave DACs: Challenges and Opportunities (Invited)**
W. Khalil[1], J. Wilson[2], B. Dupaix[1], S. Balasubramanian[1], G. Creech[3], *[1]The Ohio State University, Columbus, United States, [2]Army Research Laboratory, Washington, United States, [3]Air Force Research Laboratory, Wright-Patterson AFB, United States*

Monday, October 15th, 2012

10:45 a.m.

A.4 **Deeply Scaled E/D-mode GaN HEMTs for Submillimeter-wave Amplifiers and Mixed Signal Applications (Invited)**
K. Shinohara[1], D. Regan[1], A. Corrion[1], D. Brown[1], I. Alvarado-Rodriguez[1], M. Cunningham[1], C. Bulter[1], A. Schmitz[1], S. Kim[1], B. Holden[1], D. Chang[1], A. Margomenos[1], M. Micovic[1], V. Lee[2], P. M. Asbeck[2], *[1]HRL Laboratories, Malibu, United States, [2]University of California San Diego, La Jolla, United States*

11:15 a.m.

A.5 **MMICs and Remote Sensing Science Instruments - A Technology Success Story (Invited)**
T. C. Gaier, *Jet Propulsion Laboratory, Pasadena, United States*

11:45 a.m.
End of Session A

12:00 p.m. – 1:30 p.m.
Break for Lunch

SESSION B: GaN Power Amplifiers

1:30 p.m. – 2:30 p.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Seyed Tabatabaei, *Teramics*
Tomoya Kaneko, *NEC*

1:30 p.m.

B.1 **An S-band GaN on Si High Power Amplifier with 170W Output Power and 70% Drain Efficiency**
N. Kosaka[1], H. Uchida[1], H. Noto[1], K. Yamanaka[1], M. Nakayama[1], K. Kanaya[2], Y. Nogami[2], A. Inoue[2], Y. Hirano[2], *[1]Mitsubishi Electric Corporation, Kamakura, Japan, [2]Mitsubishi Electric Corporation, Itami, Japan*

1:50 p.m.

B.2 **160W InAlN/GaN HEMTs Amplifier at 2 GHz with Optimized Thermal Management**
S. Piotrowicz[1], O. Jardel[1], J. Jacquet[1], D. Lancereau[1], R. Aubry[1], E. Morvan[1], N. Sarazin[1], J. Dufraisse[1], C. Dua[1], M. Oualli[1], E. Chartier[1], M. Di-Forte Poisson[1], C. Gaquiere[2], S. L. Delage[1], *[1]III-V Lab, Marcoussis, France, [2]MC2-Technologies, Villeneuve d'Ascq, France*

2:10 p.m.

B.3 **A Compact 70 Watt Power Amplifier MMIC Utilizing S-band GaN on SiC HEMT Process**
S. Chen, E. Reese, T. Nguyen, *TriQuint Semiconductor, Richardson, United States*

2:30 p.m
End of Session B

Monday, October 15th, 2012

SESSION C: Heterogeneous Integration

1:30 p.m. – 3:10 p.m.
Aventine DE – Hyatt Regency La Jolla at Aventine

Chairpersons: Gilbert Dewey, *Intel*
Scott Gatley, *WIN Semiconductors*

1:30 p.m.
C.1 **Towards the Monolithic Integration of III-V Compound Semiconductors on Si: Selective Area Growth in High Aspect Ratio Structures vs. Strain Relaxed Buffer-Mediated (Invited)**
M. Cantoro[1], C. Merckling[1], S. Jiang[1,2], W. Guo[1], N. Waldron[1], H. Bender[1], B. Douhard[1], W.Vandervorst[1,3], J. Dekoster[1], R. Loo[1], M. Caymax[1], M. Heyns[1,2], *[1]imec, Leuven, Belgium, [2]Dept of Metallurgy and Materials Engineering, KULeuven, Leuven, Belgium, [3]Dept of Physics, KULeuven, Leuven, Belgium*

2:00 p.m.
C.2 **Prospects for a BiCFET III-V HBT Process**
P. J. Zampardi, M. Sun, C. Cismaru, J. Li, *Skyworks Solutions, Inc., Newbury Park, United States*

2:20 p.m.
C.3 **A Planar Switchable Capacitor with Embedded Two-Dimensional Electron System for Higher Integrations in VLSI and RFIC**
P. Dianat[1], R. W. Prusak[1], F. Quaranta[2], A. Cola[2], B. Nabet[2], *[1]Drexel University, Philadelphia, United States, [2]Institute for Microelectronics and Microsystems-Unit of Lecce, National Council of Research, Lecce, Italy*

2:40 p.m.
C.4 **RF performance potential of strained-Si, $In_{0.53}Ga_{0.47}As$, and GaSb double-gate ultra-thin-body n-FETs with Lg=10.7 nm (Invited)**
M. Luisier, *Integrated Systems Laboratory, ETH Zurich, Zurich, Switzerland*

3:10 p.m.
End of Session C

SESSION D: mm-Wave Transceivers & Building Blocks

3:30 p.m. – 5:50 p.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Hossein Hashemi, *University of Southern California*
Payam Heydari, *University of California, Irvine*

3:30 p.m.
D.1 **Design of Wide Tuning-Range mm-Wave VCOs Using Negative Capacitance**
Qiyang Wu[1], T. Quach[2], Aji Mattamana[2], S. Elabd[1], Ste ve R. Dooley[2], J. McCue[1], P. Orlando[2], G. Creech[2], W. Khalil[1], *[1]Ohio State University, Columbus, USA, [2]Air Force Research Laboratory, Wright-Patterson AFB, USA*

Monday, October 15th, 2012

3:50 p.m.

D.2 **A Highly Efficient 0.2 THz Varactor-Less VCO with -7 dBm Output Power in 130nm SiGe**
Pei-Yuan Chiang[1], O. Momeni[1,2], P. Heydari[1], [1]*University of California, Irvine, USA,* [2]*University of California, Davis, USA*

4:10 p.m.

D.3 **Compact Integration of Sub-Harmonic Resistive Mixer with Differential Double Slot Antenna in G-Band Using 50 nm InP-HEMT MMIC Process**
Y. Karandikar, H. Zirath, Yu Yan, V. Vassilev, *Chalmers University of Technology, Goteborg, Sweden*

4:30 p.m.

D.4 **Highly Integrated E-Band Direct Conversion Receiver**
M. Ferndahl[1,2], M. Gavell[1,2], M. Abbasi[1,2], H. Zirath[2,1], [1]*Gotmic AB, Goteborg, Sweden,* [2]*Chalmers University of Technology, Goteborg, Sweden*

4:50 p.m.

D.5 **60 GHz CMOS Direct-Conversion Transceiver Using Injection-Lock Oscillators (Invited)**
K. Okada, *Tokyo Institute of Technology, Tokyo, Japan*

5:20 p.m.

D.6 **Short-Millimeter-Wave CMOS Design for Ultrahigh-Speed Wireless Communication (Invited)**
M. Fujishima, *Hiroshima University, Higashi-hiroshima, Hiroshima, Japan*

5:50 p.m.

End of Session D

Monday, October 15th, 2012

SESSION E: High-Frequency Technology

3:30 p.m. – 5:50 p.m.
Aventine DE – Hyatt Regency La Jolla at Aventine

Chairpersons: Paul Rosenthal, *Boeing*
Jim Sewell, *Air Force Research Laboratory*

3:30 p.m.
E.1 **mm-Wave InP/GaAsSb DHBTs with a Novel Teflon AF Planarization and Comparison to Airbridge Process**
R. Lövblom, R. Flückiger, M. Alexandrova, C.R. Bolognesi, *ETH-Zürich, Zürich, Switzerland*

3:50 p.m.
E.2 **SiGe BiCMOS Technologies for Applications above 100 GHz (Invited)**
H. Rücker, B. Heinemann, A. Fox, *IHP, Frankfurt, Germany*

4:20 p.m.
E.3 **Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz (Invited)**
P. Chevalier[1], T. Lacave[1,2], E. Canderle[1,2], A. Pottrain[2], Y. Carminati[1], J. Rosa[1], F. Pourchon[1], N. Derrier[1], G. Avenier[1], A. Montagne[1], A. Balteanu[3], E. Dacquay[3], I. Sarkas[3], D. Celi[1], D. Gloria[1], C. Gaquiere[2], S. P. Voinigescu[3], A. Chantre[1], [1]*STMicroelectronics, Crolles, France,* [2]*IEMN, Villeneuve d'Ascq, France,* [3]*University of Toronto, Toronto, Canada*

4:50 p.m.
E.4 **Adaptability of a 280GHz SiGe BiCMOS Process for High-Frequency Commercial Applications (Invited)**
E. Preisler, J. Zheng, S. Chaudhry, Z. Yan, R. Booth, M. Y. Qamar, M. Racanelli, *TowerJazz, Newport Beach, United States*

5:20 p.m.
E.5 **THz Indium Phosphide Bipolar Transistor Technology (Invited)**
M. J. Rodwell[1], J. Rode[1], H. Chiang[1], P. Choudhary[1], T. Reed[1], E. Bloch[1], S. Daneshgar[1], B. Brar[2], H. Park[1], A. C. Gossard[1], B. Thibeault[1], W. Mitchell[1], M. Urteaga[2], Z. Griffith[2], J. Hacker[2], M. Seo[2], [1]*University of California, Santa Barbara, Santa Barbara, United States,* [2]*Teledyne Scientific Company, Thousand Oaks, United States*

5:50 p.m.
End of Session E

Technology Exhibition
Opening Reception
Pavilion
6:00 p.m. - 7:30 p.m.

Tuesday, October 16th, 2012

REGISTRATION AND BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Grand Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Pavilion

SESSION F: HEMT/FET Modeling

8:30 a.m. – 10:00 a.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Joe Gering, *RFMD*
Wolfram Stiebler, *TriQuint Semiconductor*

8:30 a.m.
F.1 **Modeling of FET Switches (Invited)**
F. Kharabi, J. Gering, J. McMacken, *RFMD, Greensboro, United States*

9:00 a.m.
F.2 **Multi-gate pHEMT Modeling for Switch Applications**
C.-J. Wei, H. Yin, O. Klimashov, Y. Zhu, D. Bartle, *Skyworks Solutions, Woburn, United States*

9:20 a.m.
F.3 **A Non Linear Electrothermal Model of AlGaN/GaN HEMT for Switch Applications**
C. Charbonniaud, A. Xiong, S. Dellier, T. Gasseling, *AMCAD Engineering, Limoges, France*

9:40 a.m.
F.4 **A Surface-Potential-Based Compact Model for Study of Non-Linearities in AlGaAs/GaAs HEMTs**
S. Khandelwal, T. Fjeldly, *Norwegian University of Science and Technology, Trondheim, Norway*

10:00 a.m.
End of Session F

SESSION G: Advanced Electro-Optical Components

8:30 a.m. – 10:10 a.m.
Aventine DE – Hyatt Regency Hotel La Jolla at Aventine

Chairpersons: Hideyuki Nosaka, *NTT Photonics Lab.*
Payam Heydari, *University of California at Irvine*

8:30 a.m.
G.1 **High-speed InP-based Mach-Zhender Modulator for Advanced Modulation Formats (Invited)**
N. Kikuchi, E. Yamada, Y. Shibata and Hiroyuki Ishii, *NTT Photonics Laboratories NTT Corporation, Kanagawa, Japan,*

Tuesday, October 16th, 2012

9:00 a.m.

G.2 **Photonics-Electronics Convergence System for High Density Inter-chip Interconnects by using Silicon Photonics (Invited)**
Y. Urino[1,2], T. Horikawa[1,3], T. Nakamura[1,2] and Y. Arakawa[1,4]
[1]*Institute for Photonics-Electronics Convergence System Technology (PECST)*
[2]*Photonics Electronics Technology Research Association (PETRA), Tsukuba, Japan*
[3]*National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan*
[4]*Institute of Industrial Science, The University of Tokyo, Tokyo, Japan*

9:30 a.m.

G.3 **100 Gb/s Optical DP-QPSK using two Surface Mount Dual Channel Modulator Drivers**
C. Steinbeiser, K. Dinh, A. Chiu, M. Coutant, O. Krutko and M. Tessaro
TriQuint Semiconductor, Richardson, Texas

9:50 a.m.

G.4 **Optoelectronic Chip Based on a Laser Integrated with a Thermoelectrophotonic Heat Pump**
X. Liu, G. Zhao, Y. Zhang and D.G. Deppe,
CREOL, College of Optics & Photonics, University of Central Florida, Orlando, FL

10:10 a.m.
End of Session G

PANEL SESSION 1: Circuit design with FEM EM simulators

Does an IC designer really need Arbitrary 3D EM Analysis?

10:30 a.m. – 12:00 p.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Moderators: Qi Zhang, *Hittite*
Jim Carroll, *AWR Corporation*

In the past, IC designers exclusively used planar EM simulators (such as Sonnet) for their IC designs because of their ease of use and computational efficiency. However, arbitrary 3D EM simulators based on the Finite Element Method (FEM) is slowly becoming more prominent in IC design. Designers now have to consider more than just planar problems in their chip, package, and even system in a package designs such as bondwires, ball-grid arrays, chip to chip transitions, and the effect of thick dielectric coatings. Having tools capable of these types of simulations are now a critical part of the design flow for MMIC designers and the FEM tool sets are steadily improving to help designers with these needs. This panel will discuss current EM tools available to IC designers today and the past and future use-models for these products. Panelist will describe how they are working to make the process of EM circuit simulation better and easier for the designer while helping them avoid mistakes and accuracy issues. Questions for the panel include:

- What type of computational speed and memory improvements have been made in the past 5 years and where will be in the next five years?
- Are the Planar class of simulators going the way of the dinosaur while the more generalized FEM tools rule?
- Where is parallel and distributed processing now and what will it look like in 5 years?
- Will any microwave design tool revolution happen in future?

Panel Members:

Rashaunda Henderson	User	*University of Texas at Dallas*
Jonathan Oakley	CST	*CST*
Lawrence Williams	HFSS	*Ansys*
Marc Petersen	EMPro	*Agilent*
John Dunn	Analyst	*AWR Corporation*

12:00 p.m.
End of Panel Session 1

12:00 p.m. – 1:30 p.m.
Break for Lunch

Technology Exhibition Lunch Pavilion
12:00 p.m. – 1:30 p.m.

SESSION H: Thermal Management

1:30 p.m. – 3:10 p.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Avram Bar-Cohen, *DARPA*
Joseph Maurer, *Booz Allen Hamilton*

1:30 p.m.
H.1 **Temperature Dependent Thermal Resistances at GaN–substrate Interfaces in GaN Composite Substrates**
J. Cho[1], Y. Li[1], D. H. Altman[2], W. E. Hoke[2], M. Asheghi[1], K. E. Goodson[1], *[1]Stanford University, Stanford, United States, [2]Raytheon Company, Waltham, United States*

1:50 p.m.
H.2 **Engineering Design of a Near Junction Thermal Transport Heat Spreader**
G. D. Mandrusiak[1], S. E. Weaver[1], D. Y. Lin[1], E. A. Browne[1], M. F. Aimi[1], O. C. Boomhower[1], R. Vetury[2], *[1]General Electric Global Research, Niskayuna, United States, [2]RF Micro Devices, Greensboro, United States*

2:10 p.m.

H.3 **GaN HEMT Junction Temperature Dependence on Diamond Substrate Anisotropy and Thermal Boundary Resistance**

H. C. Nochetto[1], N. R. Jankowski[2], A. Bar-Cohen[3], *[1]General Technical Services, LLC, Wall, United States, [2]U.S. Army Research Laboratory, Adelphi, United States, [3]Defense Advanced Research Projects Agency, Arlington, United States*

2:30 p.m.

H.4 **Device Scale Heat Removal for High Power Density GaN Devices**

A. Bhunia, A. Brackley, C. Nguyen, B. Brar, *Teledyne Scientific Company, Thousand Oaks, United States*

2:50 p.m.

H.5 **Diamond Materials for GaN HEMT Near Junction Heat Removal (Breaking News Paper)**

R. Sandhu[1], V. Gambin[1], B. Poust[1], I. Smorchkova[1], G. Lewis[1], R. Elmadjian[1], D. Li[1], C. Geiger[1], B. Heying[1], M. Wojtowicz[1], A. Oki[1], T. Feygelson[2], K. Hobart[2], E. Bozorg-Grayeli[3], K. Goodson[3],
[1]Northrop Grumman Aerospace Systems, CA
[2]Naval Research Lab, Washington, DC
[3]Stanford University, CA

3:10 p.m.

End of Session H

SESSION I: RF CMOS Circuits

1:30 p.m. – 3:00 p.m.

Aventine DE – Hyatt Regency La Jolla at Aventine

Chairpersons: Donald Kimball, *MaXentric Technologies*
Harris Moyer, *Hughes Research Lab*

1:30 p.m.

I.1 **A Watt-class Digital Transmitter with a Voltage-Mode Class-S Power Amplifier and an Envelope Delta-sigma Modulator for 450 MHz band**

S. Hori[1], A. Wentzel[2], M. Hayakawa[1], W. Heinrich[2], K. Kunihiro[1], *[1]NEC, Kawasaki, Japan, [2]Ferdinand-Braun-Institut, Berlin, Germany*

1:50 p.m.

I.2 **A Compact Fully Integrated High-Efficiency 5GHz Stacked Class-E PA in 65nm CMOS based on Transformer-based Charging Acceleration**

J. Chen, R. Bhat, H. Krishnaswamy, *Columbia University, New York, United States*

2:10 p.m.

I.3 **An Envelope-Tracking CMOS-SOS Power Amplifier With 50% Overall PAE and 29.3 dBm Output Power for LTE Applications (Breaking News Paper)**

M. Hassan[1], C. Olson[2], D. Kovac[2], J. Yan[1], D. Nobbe[2], D. Kelly[3], P. Asbeck[1], and L. Larson[4],
[1]University of California at San Diego, CA
[2]Peregrine Semiconductor, Arlington Heights, IL
[3]Peregrine Semiconductor, San Diego, CA
[4]Brown University, RI

2:30 p.m

I.4 **High-Performance CMOS RF Front-End Design Techniques for Adaptive and Cognitive Radios (Invited)**

L. Larson[1], P. Gudem[3], C. Thomas[2], S. Abdelhalem[2], [1]*Brown University, Providence, United States*, [2]*UCSD, La Jolla, United States*, [3]*Qualcomm, Inc, San Diego, United States*

3:00 p.m

End of Session I

PANEL SESSION 2:
Is Diamond the Answer for High Power Density GaN?

3:30 p.m. – 5:00 p.m.

Aventine, ABC - Hyatt Regency La Jolla at Aventine

Moderators: Avram Bar-Cohen, *DARPA*
Bruce Green, *Freescale Semiconductor*

As power densities in electronic and photonic devices and components increase, packaging and cooling impose a ceiling on electrical performance. Overcoming such barriers requires the engineering of thermal management techniques within close proximity to the heat source. This requires near-channel – or, in the case of GaN HEMTs, near-junction – techniques. This panel addresses several questions in this area: In what ways can diamond be integrated with high-power GaN devices? What is necessary from a metrology standpoint to support the integration of diamond? What about alternatives to diamond such as SiC microchannel cooling? Can diamond and microchannel cooling complement one another? Is the benefit of diamond or microchannel cooling worth the cost and complexity?

Panel Members:

P.C. Chao	***BAE Systems***
David Fanning	***TriQuint Semiconductor***
Ken Goodson	***Stanford University***
Nicholas Jankowski	***Army Research Laboratory***
Rama Vetury	***RF Micro Devices***
Stanton Weaver Jr.	***General Electric Global Research***

12:00 p.m.

End of Panel Session 2

Wednesday, October 16th, 2012

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 12:00 p.m.
Registration –Grand Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Pavilion

SESSION J: Design Techniques for High-Efficiency Power Amplifiers

8:30 a.m. – 9:40 a.m.
Aventine ABC – Hyatt Regency La Jolla at Aventine

Chairpersons: Brian Hughes, *HRL*
Colombo Bolognesi, *ETH-Zürich*

8:30 a.m.
J.1 **Doherty Power Amplifier Design in Gallium Nitride Technology using Nonlinear Vector Network Analyzer and X-parameters**
T.S. Nielsen[1], M. Dieudonné[1], C. Gillease[2], and D.E. Root[2]
[1] Agilent Technologies, Inc., Rotselaar, B-3110 Belgium,
[2] Agilent Technologies, Inc., Santa Rosa, California, CA95403, United States

8:50 a.m.
J.2 **A High-Efficiency Class-F MMIC Power Amplifier at 4.0 GHz using AlGaN/GaN Technology**
V. Zomorrodian, U.K. Mishra, R.A. York, *University of California, Santa Barbara, CA93106, United States*

9:10 a.m.
J.3 **Wideband PA Design: The "Continuous" Mode of Operation (Invited)**
P.J. Tasker, V. Carruba, P. Wright, J. Lees, J. Benedikt, S. Cripps, *Center for High-Frequency Engineering, Cardiff University, United Kingdom*

SESSION K: mm-wave Amplifiers

8:30 a.m. – 10:10 a.m.
Aventine DE – Hyatt Regency La Jolla at Aventine

Chairpersons: Marc Rocchi, *OMMIC*
Frank E. van Vliet, *TNO*

8:30 a.m.
K.1 **A 220 GHz InP HBT Solid-State Power Amplifier MMIC with 90 mW P_{out} at 8.2 dB Compressed Gain**
T.B. Reed[1], M. Rodwell[1], Z. Griffith[2], P. Rowell[2], A. Young[2], M. Urteaga[2], M. Field[2]
[1]Dept. of ECE, Univ. of California, Santa Barbara, CA, USA
[2]Teledyne Scientific and Imaging, Thousands Oaks, CA, USA

8:50 a.m.
K.2 **Dual-Output Stacked Class-EE Power Amplifiers in 45nm SOI CMOS for Q-Band Applications**
A. Chakrabarti, J. Sharma, H. Krishnaswamy
Dept. of EE, Columbia Univ., New York, NY, USA

9:10 a.m.
K.3 **A 60 GHz Variable Gain Amplifier with a Low Phase Imbalance in 0.18 um SiGe BiCMOS Technology**
C.W. Byeon, I.S. Song, S.J. Cho, H.Y. Kim, C. Lee, C.S. Park
IREC, KAIST, Daejeon, Republic of Korea

Wednesday, October 16th, 2012

9:30 a.m.

K.4 **F-Band Bidirectional Amplifier using 75-nm InP HEMT's**
S. Shiba, M. Sato, T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, N. Hara
Fujitsu Limited, Fujitsu Laboratories Ltd.,Kanagawa, Japan

9:50 a.m.

K.5 **160-270 GHz InP HEMT MMIC Low-Noise Amplifiers**
M. Varonen[1], P. Larkoski[2], A. Fung[1], L. Samoska[1], P. Kangaslahti[1], T. Gaier[1], R. Lai[3], S. Sarkozy[3]
[1]JPL, Cal. Inst.Of Techn., Pasadena, CA, USA
[2]Dept. of Physics, Stanford Univ., Stanford, CA, USA
[3]Northrop Grumman Corp., Redondo Beach, CA, USA

10:10 a.m
End of Session K

SESSION L: High Power Technologies

10:30 a.m. – 11:50 a.m.
Aventine, ABC - Hyatt Regency La Jolla at Aventine

Chairpersons: Bruce Green, *Freescale Semiconductor*
Jim Sewell, *Air Force Research Laboratory*

10:30 a.m.

L.1 **Back to the Future: An all-NMOS SiC Linear Voltage Regulator for High-Temperature Applications**
J. Valle-Mayorga, A. Rahman, and H. A. Mantooth
Department of Electrical Engineering, University of Arkansas, Fayetteville, United States

10:50 a.m.

L.2 **Simulation Study and Reduction of Reverse Gate Leakage Current for GaN HEMTs**
Y. Yamaguchi[1], K. Hayashi[1] T. Oishi[1], H. Otsuka[1], T. Nanjo[2], K. Yamanaka[1], M. Nakayama[1], Y. Miyamoto[3]
[1]Information Technology R&D Center, Mitsubishi Electric Corporation, Kanagawa, Japan
[2]Advanced Technology R&D Center, Mitsubishi Electric Corporation, Hyogo, Japan,
[3]Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan

11:10 a.m.

L.3 **Degradation Characteristics of High-Voltage AlGaN/GaN-on-Si Heterostructure FETs under DC Stress**
Shinhyuk Choi, Jae-Gil Lee, Hoonsang Yoon, Ho-Young Cha, and Hyungtak Kim, *School of Electrical Engineering, Hongik University, Seoul, Korea*

11:30 a.m.

L.4 **Determination of the Reliability of AlGaN/GaN HEMTs through Trap Detection using Optical Pumping**
David Cheney[1], Rick Deist[2], Brent Gila[2], Fan Ren[3], and Steve Pearton[2], [1] *Electrical & Computer Engineering, University of Florida, Gainesville, United States,* [2]*Material Science & Engineering, University of Florida, Gainesville, United States,* [3]*Chemical Engineering, University of Florida, Gainesville, United States*

11:50 a.m.
End of Session L

SESSION M: Receiver Circuits

10:30 a.m. – 11:50 a.m.
Aventine DE – Hyatt Regency La Jolla at Aventine

Chairpersons: Gilberto De la Rosa, ANADIGICS Inc.
Kazuya Yamamoto, Mitsubishi Electric

10:30 a.m.

M.1 **Highly Linear Gallium Nitride MMIC LNAs**
O. Axelsson, K. Andersson
Chalmers University of Technology, Göteborg, Sweden

10:50 a.m.

M.2 **PHEMT-Based Ultrawideband Low Noise Amplifier with Room-Cryogenic Temperature Operability**
H. Vemuri[1], S. Velicu[1], A. S. Gilmore[1], C. Grein[1], A. Mattamana[2], T. Quach[2], P. Orlando[2], C. Campbell[3]
[1]*EPIR Technologies, Inc., Bolingbrook, IL*
[2]*WPAFB, Dayton, OH*
[3]*TriQuint Semiconductors, Richardson, TX*

11:10 a.m.

M.3 **A 20 GHz Low Phase Noise Signal Source Using VCO and Mixer in InGaP/GaAs HBT**
S. Lai, M. Bao, D. Kuylenstierna, H. Zirath
Chalmers University of Technology, Gothenburg, Sweden

11:30 a.m.

M.4 **A Novel Electrostatic Discharge (ESD) Protection Circuit in D-Mode pHEMT Technology**
Q. Cui[1, 2], S. Zhang[1], Y. Zhao[1], B. Hou[1], J. J. Liou[2]
[1]*Analog Devices, Wilmington, MA*
[2]*University of Central Florida, Orlando*

11:50 a.m.
End of Session M

Wednesday, October 16th, 2012

SESSION N: Power Amplifier Modules

1:30 p.m. – 2:50 p.m.
Aventine ABC – Hyatt Regency Hotel La Jolla
Chairpersons: Steve Huettner, *Nuvotronics LLC*
Qi Zhang, *Hittite Microwave CO*

1:30 p.m.
N.1 **Linearization of a Spatially-Combined X-Band 100-W GaAs FET Power Amplifier System with Predistortion Linearizer**
Y. Chung, B. C. Deckman, M. P. DeLisio, *Wavestream Corp, San Dimas, United States*

1:50 p.m.
N.2 **A High Efficiency 780 MHz GaN Envelope Tracking Power Amplifier**
J. J. Yan[2], P. Theilmann[1], D. F. Kimball[1],
[1]*MaXentric Technologies, La Jolla, United States,*
[2]*University of California, San Diego, La Jolla, United States*

2:10 p.m.
N.3 **S-band Class-F Power Amplifier with Integrated Switched Mode Power Supply**
G. van der Bent[1], P. de Hek[1], F. E. van Vliet[1], S. Geurts[2], H. Brouzes[2],
[1]*TNO, The Hague, Netherlands,*
[2]*Thales Nederland B.V., Hengelo, Netherlands*

2:30 p.m.
N.4 **A K-Band 5W Doherty Amplifier MMIC Utilizing 0.15um GaN on SiC HEMT Technology**
C. F. Campbell, K. Tran, M. Kao, S. Nayak, *TriQuint Semiconductor, Richardson, United States*

2:50 p.m
End of Session N

Wednesday, October 16th, 2012

SESSION O: High Speed Mixed-Signal Circuits

1:30 p.m. – 2:40 p.m.
Aventine DE – Hyatt Regency Hotel La Jolla

Chairpersons: Myung-Jun Choe, *Teledyne*
Greg Creech, *AF Research Lab.*

1:30 p.m.
O.1 **InP HBT/Si CMOS-based 13-Bit 1.33Gsps Digital-to-Analog Converter with >70 dB SFDR (Invited)**
B. Oyama, D. Ching, K. Thai, A. Gutierrez-Aitken, N. Cohen, D. Scott, K. Hennig, E. Kaneshiro, P. Nam, J. Chen, P. Chang-Chien, V.J. Patel[1], *Northrop Grumman Aerospace Systems, Redondo Beach, CA,* [1]*Air Force Research Labs, Wright-Patterson AFB, Dayton, OH*

2:00 p.m.
O.2 **A High IIP3, 50-GSamples/s Track and Hold Amplifier in 0.25 um InP HBT Technology**
S. Daneshgar[1], Z. Griffith[2] and M. Rodwell[1]
[1]*Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA*
[2]*Teledyne Scientific and Imaging, Thousand Oaks, CA*

2:20 p.m.
O.3 **A 1.8 V SiGe BiCMOS Cable Equalizer with 40-dB Peaking Control up to 60GHz**
I. Sarkas and S. P. Voinigescu, *Department of Electrical and Computer Engineering, University of Toronto, Canada*

2:40 p.m.
End of Session O

SESSION P: Breaking News Papers

3:30 p.m. – 5:10 p.m.
Aventine ABC – Hyatt Regency Hotel La Jolla

Chairpersons: Sorin Voinigescu, *University of Toronto*
Francois Colomb, *Raytheon*

3:30 p.m.
P.1 **A 22.4 dBm Two-Way Wilkinson Power-Combined Q-Band SiGe Class-E Power Amplifier With 23% Peak PAE**
K. Datta, J. Roderick, and H. Hashemi, *University of Southern California, Los Angeles, CA*

3:50 p.m.
P.2 **Full ETSI E-Band Doubler, Quadrupler and 24 dBm Power Amplifier**
M. Rodriguez[1], J. Tarazi[1], A. Dadello[1], E. Convert[1], M. McCulloch[1], S. Mahon[1], S. Hwang[1], R. Mould[1], A. Fattorini[1], A. Young[1], J. Harvey[1], A. Parker[2], M. Heimlich[2] and W.-K. Wang[3],
[1]*Sydney Design Centre, Macom Tech. Solutions, Australia*
[2]*Macquarie University, Australia*
[3]*WIN Semiconductor, Taiwan*

Wednesday, October 16th, 2012

4:10 p.m.

P.3 **A Fundamental Frequency 143-152 GHz Radar Transceiver with Built-in Calibration and Self-Test**

I. Sarkas[1], M. Girma[2], J. Hasch[2], T. Zwick[3], S.P. Voinigescu[1],
[1]*University of Toronto, Canada*
[2]*Robert Bosch GmbH, Germany*
[3]*Institut fur Hochfrequenztechnik und Elektronik, Germany*

4:30 p.m.

P.4 **A High Gain 600 GHz Amplifier TMIC Using 35 nm Metamorphic HEMT Technology**

A. Tessmann, A. Leuther, H. Massler, M. Seelmann-Eggebert,
Fraunhofer Institute for Applied Solid State Physics (IAF), Germany

4:50 p.m.

P.5 **High Performance Ka-Band VPIN Limiters**

R. Santhakumar and D. Allen, *TriQuint Semiconductor, Texas*

5:10 p.m.

End of Session P

Close of Symposium

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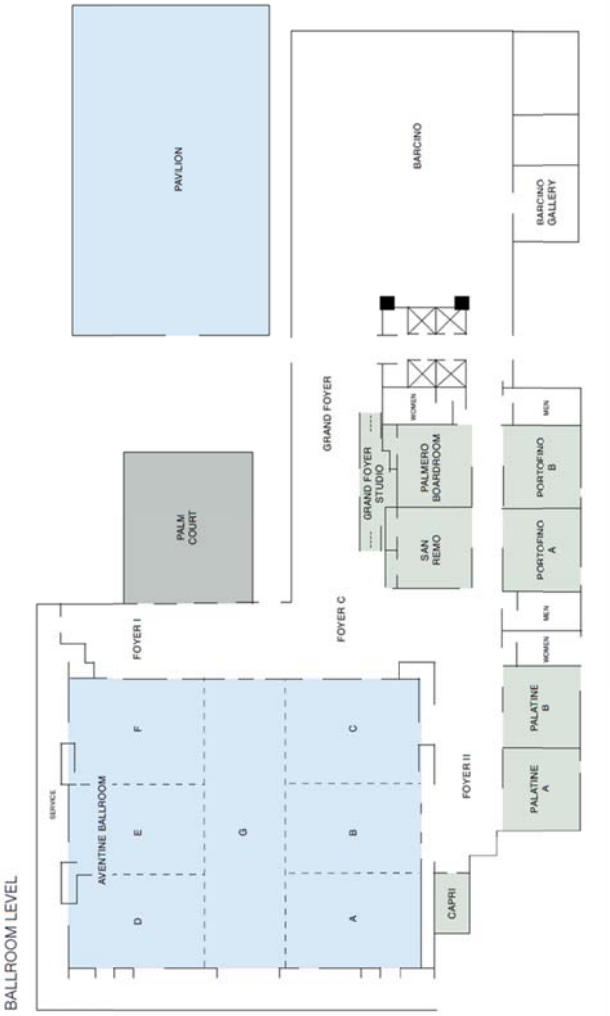

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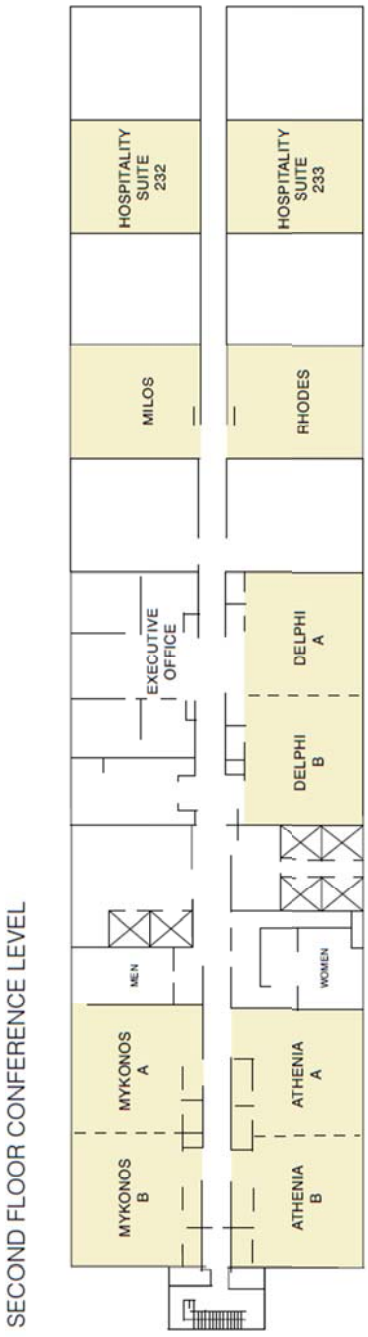

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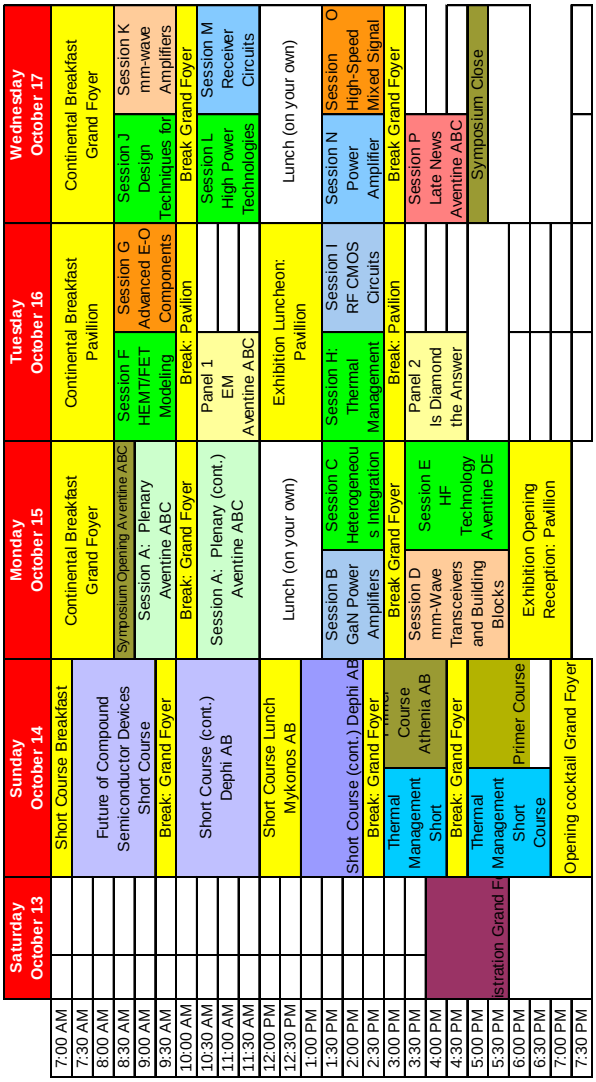

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