



## **Program Update August 16, 2004**

**“Late News Papers” added to schedule**

**(Note: Not included in printed advance program)**

**Late News Papers:**

**Tuesday 8:00 a.m. Session E:**

- E.3L A 2-Bit 20 Gbps InP HBT A/D Converter for Optical Communications, Zheng Guo, et. al**
- E.4L A Fast Low-Power 4x4 Switch IC Using InP HEMTs for 10-Gbit/s Systems, Hideki Kamitsuna, et. al.**
- E.5L A 49-Gb/s, 7-Tap Transversal Filter in 0.18 $\mu$ m SiGe BiCMOS for Backplane Equalization, Altan Hazneci, et. al**
- E.6L A 60-Gb/s 0.7-V 10-mW Monolithic Transformer-Coupled 2:1 Multiplexer in 90 nm CMOS, Daniel Kehrer, et. al.**

**Tuesday 10:20 a.m. Session G:**

- G.4L A 20 GHz Low Noise Amplifier with Active Balun in a 0.25  $\mu$ m SiGe BICMOS Technology  
Brian Welch, et.al**
- G.5L A 90-GHz InP-HEMT Lossy Match Amplifier with 20-dB Gain Using a Broadband Matching Technique, Y. Inoue, et. al**

**Tuesday 1:20 p.m. Session H:**

- H.5L A Low Power (45mW/latch) Static 150GHz CML Divider  
Donald A. Hitko, et. al**
- H.6L 120-GHz Tx/Rx Chipset for 10-Gbit/s Wireless Applications Using 0.1- $\mu$ m-gate InP HEMTs, Toshihiko Kosugi, et. al**



**2004**  
**26<sup>th</sup> IEEE COMPOUND**  
**SEMICONDUCTOR IC**  
**SYMPOSIUM**  
(Formerly IEEE GaAs IC Symposium)

# Program

**Presenting:**

**Compounding Your Chips  
in Monterey**

**Introducing:**  
**Compound Semiconductor Week 2004**  
A co-location of the IEEE CSIC Symposium and CS-MAX

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**October 24-27, 2004**  
**Portola Plaza Hotel**  
**Monterey, CA, USA**



**SPONSORED BY**  
**The IEEE Electron Devices Society**

**Technically Co-Sponsored by:**  
**The IEEE Microwave Theory and**  
**Techniques Society, and**  
**The IEEE Solid-State Circuits Society**

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## SYMPOSIUM

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### **SATURDAY, OCTOBER 23, 2004**

REGISTRATION (Short Course & Primer Course Only)

### **SUNDAY, OCTOBER 24, 2004**

REGISTRATION (Short Course & Primer Course Only)

#### **Continental Breakfast for Short Course**

SHORT COURSE 1: "Power Amplifier Technologies and Markets for Compound Semiconductors"

SHORT COURSE 2: "High Speed Data Converters"

Reliability of CS (ROCS) Workshop (Registration, Workshop, and Lunch)

#### **Short Course Lunch**

REGISTRATION for Symposium (and Primer Course until 4:00)

PRIMER COURSE: "Basics of Compound Semiconductor ICs"

#### **Symposium Opening Reception**

### **MONDAY, OCTOBER 25, 2004**

REGISTRATION

#### **Continental Breakfast**

SYMPOSIUM OPENING

SESSION A: Plenary Session

SESSION B: Mixed Signal Circuits and Technologies

SESSION C: High Power Amplifiers Below 5 GHz

PANEL SESSION 1: What Technology Gives the Ultimate High Speed Data Converter?

PANEL SESSION 2: Integrated PA Module Packaging Shoot-out

#### **Symposium Party**

### **TUESDAY, OCTOBER 26, 2004**

REGISTRATION

#### **Continental Breakfast**

SESSION D: HBTs

SESSION E: Optical Systems Building Blocks

SESSION F: FETs

SESSION G: High Performance MMIC Power Amplifiers

PANEL SESSION 3: III-V Foundries Pure-play vs Captive

SESSION H: Novel Signal Generation and Switching ICs

SESSION I: Advanced Si Transceiver ICs

SESSION J: High Power Technologies

#### **CS-Week 2004 Technology Exhibition Opening Reception**

CS-Week 2004 Technology Exhibition

### **WEDNESDAY, OCTOBER 27, 2004**

REGISTRATION

#### **Continental Breakfast**

CS-Week Technology Exhibition

SESSION K: Beyond 100 GB/s

SESSION L: Integration

SESSION M: CMOS, GaAs and InP for 40GB/s

SESSION N: MMIC Mixers and Multipliers

#### **CS-Week 2004 Technology Exhibition Luncheon**

PANEL SESSION 4: When will 40GB/s Market Materialize?

PANEL SESSION 5: mmW Technology Free-For All

SESSION O: Modeling

SESSION P: Millimeter Wave MMICs

#### **Close of Symposium**

Visit us on the World-Wide Web at: <http://www.csics.org/>

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## AT A GLANCE

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### Saturday

6:00 p.m.-8:00 p.m. Portola Lobby - MCC

### Sunday

7:30 a.m.-8:30 a.m. Portola Lobby - MCC

**7:30 a.m.-8:30 a.m. Lower Atrium - PPH**

8:30 a.m.-3:30 p.m. Portola Room – PPH

8:30 a.m.-3:30 p.m. Redwood Room - PPH

8:00 a.m.-5:00 p.m. De Anza III - PPH

**11:50 a.m.-1:10 p.m. Lower Atrium - PPH**

3:00 p.m.-8:00 p.m. Portola Lobby - MCC

4:00 p.m.-7:00 p.m. Portola Room - PPH

**5:30 p.m. - 8:30 p.m. De Anza Foyer and De Anza I - PPH**

### Monday

7:00 a.m.-5:00 p.m. Portola Lobby - MCC

**7:00 a.m.-8:00 a.m. De Anza Foyer - PPH**

8:00 a.m.-8:30 a.m. De Anza I & II - PPH

8:30 a.m.-12:00 p.m. De Anza I & II - PPH

1:20 p.m.-3:10 p.m. De Anza I - PPH

1:20 p.m.-3:10 p.m. De Anza II - PPH

3:40 p.m.- 5:10 p.m. De Anza I – PPH

3:40 p.m.- 5:10 p.m. De Anza II - PPH

**7:00 p.m.-10:00 p.m. De Anza III - PPH**

### Tuesday

7:00 a.m.-5:00 p.m. Portola Lobby - MCC

**7:00 a.m.-8:00 a.m. De Anza Foyer - PPH**

8:00 a.m.-9:50 a.m. De Anza I - PPH

8:00 a.m.-9:50 a.m. De Anza II - PPH

10:20 a.m.-12:10 p.m. De Anza I - PPH

10:20 a.m.-12:10 p.m. De Anza II - PPH

1:20 p.m.-3:10 p.m. De Anza I - PPH

1:20 p.m.-3:10 p.m. De Anza II - PPH

3:40 p.m.-5:10 p.m. De Anza I - PPH

3:40 p.m.-5:10 p.m. De Anza II - PPH

**5:00 p.m.-7:00 p.m. Serra Ballroom – MCC**

5:00 p.m.-8:00 p.m. Serra Ballroom – MCC

### Wednesday

7:00 a.m.-12:00 p.m. Portola Lobby - MCC

**7:00 a.m.-8:00 a.m. De Anza Foyer - PPH**

7:30 a.m.-4:00 p.m. Serra Ballroom – MCC

8:00 a.m.-10:00 a.m. De Anza I - PPH

8:00 a.m.-10:00 a.m. De Anza II - PPH

10:20 a.m.-12:00 a.m. De Anza I - PPH

10:20 a.m.-12:00 a.m. De Anza II - PPH

**11:40 a.m.-1:00 p.m. Serra Ballroom - MCC**

1:00 p.m.-2:30 p.m. De Anza I - PPH

1:00 p.m.-2:30 p.m. De Anza II - PPH

3:00 p.m.-4:30 p.m. De Anza I - PPH

3:00 p.m.-4:30 p.m. De Anza II - PPH

**5:00 p.m.**

MCC –Monterey Conference Center, PPH-Portola Plaza Hotel

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## CHAIRMAN'S MESSAGE

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On behalf of the organizing committee and the IEEE Electron Devices Society, the Microwave Theory and Techniques Society, and the Solid-State Circuits Society, I invite you to be a part of the 2004 IEEE Compound Semiconductor IC Symposium (CSICS), formerly the IEEE GaAs IC Symposium. This year's symposium will be held October 24-27 in stunning Monterey, California at the Portola Plaza Hotel (formerly the Double Tree Hotel). For those who have not heard, the IEEE GaAs IC Symposium changed its name to IEEE Compound Semiconductor IC Symposium in 2004 to better reflect the breadth of technologies it embraces. CSICS retains the same history, committee structure and integrity it has built over the last 26 years. We feel confident that this change has enabled us to continue and grow the excellent tradition everyone has come to expect.



The CSICS has become the preeminent international forum on developments in integrated circuit technologies using GaAs, InP, SiGe, GaN, SiC and other compound semiconductor devices. Our strong technical program brings the latest advances in high-frequency and high-speed circuits and technology. The program includes papers from both commercial and newly emerging military applications.

This year we are offering two short courses for the price of one. They cover the current hot topics of Power Amplifier Technologies and High Speed Data Converters and are taught by leading experts from industry and the government. In addition, our Primer Course is an excellent tutorial presented within the context of this year's Symposium content.

The big news this year is our co-location with CS-MAX in Monterey. CS-MAX offers a strong manufacturing oriented technical program and an exhibition background with wide breadth. The combined event is called Compound Semiconductor Week 2004 (CS-Week 2004) and features the separate and respective technical programs of CSICS and CS-MAX with one unified CS-Week 2004 Technology Exhibition.



We are providing several social events to allow interaction with colleagues. Events include the Sunday Evening Opening Reception, the Monday evening Symposium Theme Party, the Tuesday CS-Week 2004 Technology Exhibition Opening Reception and on Wednesday the CS-Week 2004 Technology Exhibition Luncheon.

Finally, I would like to announce the winners of our Seventh **Outstanding Paper Award from the 2003 Symposium**. They are *M. Sokolich, et al*, for their paper titled "*InP HBT Integrated Circuit Technology with Selectively Implanted Subcollector and Regrown Device Layers*", from HRL Laboratories LLC.

We hope you'll join us for Compound Semiconductor Week 2004 and contribute to the advancement of our industry!

Cheers,  
Brad Nelson, Chairman 2004 IEEE CSICS

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# CORPORATE BENEFACTORS

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This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support of the Symposium by making contributions towards the cost of some of our social events. Links to our corporate benefactors appear on our symposium website: [www.csics.org](http://www.csics.org)

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. If your company is interested in participating, please contact the Symposium Chair, Brad Nelson at 408-616-5449. Opportunities for contributions at all levels are still available.

As of this printing the Corporate Benefactors for the 2004 Compound Semiconductor IC Symposium are as follows.

General Benefactors:



Coffee Break or Breakfast:



Theme Party (Hors D'Oeuvres or Dessert) or Opening Reception:



Special Benefactors:

The Symposium Web Site [www.csics.org](http://www.csics.org) has become a critical tool for the dissemination of information for prospective attendees of the Symposium. Every year, the web site must be updated and maintained to effectively serve this purpose. We would like to acknowledge the following benefactor for providing the Symposium web site support for the 2004 CSICS:



Special publicity for the CSIC Symposium and CS-Week 2004 is being provided by Compound Semiconductor Magazine:



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# GENERAL INFORMATION

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**IEEE 26th Compound Semiconductor  
IC Symposium  
Oct 24-27th, 2004  
Portola Plaza Hotel  
(formerly Double Tree Hotel)  
Monterey, California**

## REGISTRATION

	<u>Advance</u> (Received by Sept. 22)	<u>Regular</u> (After Sept 22 or on site)
<b>Symposium Registration</b>		
IEEE Member	\$480	\$530
Non-IEEE	\$530	\$600
Student	\$200	\$250
<b>Special 1-day Registration</b> (sessions and digest only, no social activities)		
IEEE Member	\$250	\$300
Non-IEEE	\$300	\$350
<b>Short Course</b>		
Student Registration	\$200	\$300
<b>Primer Course</b>		
Student Registration	\$75	\$75
<b>Technical Digest Only</b>	\$75	\$75
<b>Short Course Notes Only</b>	\$100	\$100
<b>Digest CD ROM Only</b>	\$100	\$100
<b>Primer Course Notes Only</b>	\$50	\$50
<b>Extra Reception Ticket</b>	\$30	\$30
<b>Extra Theme Party Ticket</b>	\$75	\$75

The full Symposium registration fee includes: attendance at all technical sessions and panels; one copy of the Technical Digest and CDROM; continental breakfasts; and morning and afternoon coffee breaks. Also included are admittance to: the Sunday Opening Reception; the CS-Week Technology Exhibition Opening Reception on Tuesday and CS-Week technology Exhibition lunch on Wednesday; all exhibits; and the exciting Monday evening Theme Party. The special 1-day registration fee, however, does not include the Reception or Theme Party. Additional copies of the Technical Digest and of the Short Course Notes will be available for purchase at the Symposium.

For **ADVANCE REGISTRATION** please visit the following website:

<http://www.vipmeetings.com/conferences/csweek2004.html>

or complete the enclosed Advance Registration Form with your remittance of the appropriate fee (check or credit card) **BY Sept 22nd, 2004** to:

Registrar, 2004 IEEE Compound Semiconductor IC Symposium  
c/o VIP Meetings & Conventions  
1515 Palisades Dr. Suite I  
Pacific Palisades, CA 90272 USA  
Tel: (310) 459-0600 or (800) 926-3976  
FAX (310) 459-0605

email: [reservations@vipmeetings.com](mailto:reservations@vipmeetings.com)

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency traveler's checks, or international money order. Checks must be made payable to "VIP Meetings & Conventions" and must be encoded with the bank number, account number, and check number. Credit cards and wire transfers may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

**We urge you to pre-register** to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

### **Registration Center:**

The Symposium Registration Center is located in the Symposium Hotel on Saturday through Wednesday. The operating hours will be as follows:

#### Short & Primer Course Registration only

Saturday, October 23	6:00 p.m. - 8:00 p.m.
Sunday, October 24	7:30 a.m. - 8:30 a.m.
Sunday, October 24	3:00 p.m. - 4:00 p.m.(Primer)

#### Symposium Registration

Sunday, October 24	5:00 p.m. - 8:00 p.m.
Monday, October 25	7:00 a.m. - 5:00 p.m.
Tuesday, October 26	7:00 a.m. - 5:00 p.m.
Wednesday, October 27	7:00 a.m. - 12:00 noon

### **Refund Policy:**

Please note that after Sept. 22nd, 2004, your Advance Registration fee, Short Course fee, Primer Course fee, and fees for additional Symposium Technical Digest, or Reception/Party ticket fees are not refundable. Full refunds less \$100 handling fee will be granted for cancellations received in writing by Sept. 22nd, 2004. The letter to the Symposium Registrar (see address at VIP Meetings above) requesting the refund should state the preregistrant's name and to whom the refund check should be made payable. All refunds will be processed after the Symposium. **NO PRE-REGISTRATION REFUNDS WILL BE GRANTED AFTER Sept 22, 2004.**

# ACCOMMODATIONS

## Hotel Reservations:

A block of rooms has been reserved at a special discounted group rate for Symposium and CS Week participants at our headquarters hotel, the Portola Plaza Hotel at Monterey Bay (formerly the DoubleTree Monterey). A deluxe hotel located in the heart of the Monterey Bay overlooking scenic Fisherman's Wharf with 17 world-class golf courses and the world's best aquarium nearby. The hotel is attached to the Monterey Conference Center and is only 4 miles from the Monterey Peninsula Airport. San Jose International Airport is approximately 60 miles north of Monterey.

A major renovation was completed in 2003. The updated and spacious guest rooms include: remote control cable TV with movies and video games, a phone with voicemail and data port, iron & ironing board, and coffee maker with complimentary coffee. Bathroom amenities include Neutrogena bath products and a hair dryer. Internet access is available in every guestroom for a discounted rate of \$5 per day for CS Week attendees. Hotel guests can enjoy complimentary access to the Health Club facilities, including fitness room with Nautilus equipment, heated outdoor pool, Jacuzzi, and spa. The Spa on the Plaza offers a variety of professional services that include Yoga classes, massages and facials. The hotel offers two restaurants including Peter B's Brewpub, Monterey's only microbrewery, and The California Grill serving breakfast, lunch and dinner.

Hotel Address/Rate Information:  
Portola Plaza Hotel at Monterey Bay  
Two Portola Plaza  
Monterey, CA 93940

CS Week Group Rate: \$169 single or double  
Prevailing Gov Rate\*: \$94 single or \$124 double  
\*Prevailing government rate is available for bonafide U.S. government employees.  
Room Tax (not included in rate): 10.05%  
Rollaway bed charge: \$25 per day  
Discount Parking Rates: \$10 Self-Parking / \$12 Valet Parking

To make your Hotel Reservation:  
Please call VIP Meetings & Conventions at (800) 926-3976 or (310) 459-0600 or visit our website  
[www.vipmeetings.com/conferences/csweek2004.html](http://www.vipmeetings.com/conferences/csweek2004.html) . Please do not call the hotel direct (they will refer you back to VIP) or any regional hotel chain 800 number, since they will NOT be aware of our special arrangements. For any questions, email VIP at [reservations@vipmeetings.com](mailto:reservations@vipmeetings.com).

We ask you to please support your Symposium and more fully enjoy all the activities by staying at our official headquarters hotel. The Symposium relies on attendees staying at the Portola Plaza Hotel to reduce the costs of the meeting rooms. To guarantee room and rate availability, room reservations should be made as soon as possible, and no later than Wednesday, September 22, 2004. After this date, rate and rooms will be on space available basis. Reservations are honored on a first-come, first-served basis.

All requests for reservations will receive a reservation acknowledgement from VIP Meetings & Conventions within one business day. The hotel's phone and fax number and additional

information will be printed on the acknowledgment. Hotel's cancellation policy is 48 hours prior to arrival. If you need to cancel, please contact VIP Meetings at the numbers above.

## **TRANSPORTATION**

### **Special Airfares:**

Special discounted airfares for the 2004 CSICS Symposium have been negotiated by IEEE Travel Services. Discounts are as high as 20% off the lowest published airfares with Continental, Southwest and United Airlines.

If Saturday night stays or super-saver airfares are not applicable, deeply discounted airfares are available. Discount code A606098 entitles attendees to receive special rates that have also been negotiated with Avis Rental Car Company, Budget X520000, Hertz Corporate Code 61368/Permission Code 937661, and Enterprise NA24IE1.

Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 732 562 5387. Or, you may visit their on-line travel service web site at <http://www.ieeetravelonline.org>. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Or you can e-mail your request to [travel-team@ieee.org](mailto:travel-team@ieee.org).

You may also fax your requirements to the IEEE Travel Services at +1 732 562 8815. When faxing, please be sure to include your travel dates, departure, and return times, and phone and fax numbers. A Travel Counselor will contact you promptly.

### **Airport Transportation:**

The Monterey Peninsula Airport, serving one of the world's favorite destinations for both business and pleasure, offers commercial service with convenient connecting flights to and from anywhere in the world. Or you can fly into the area's major airports, San Jose and San Francisco, and take the scenic drive to Monterey.

#### **Driving Directions:**

*From Monterey Peninsula Airport/Highway 68 from Salinas:*

Take the Monterey Fisherman's Wharf exit, at first light turn right onto Aguajito, turn left onto Del Monte, at third light get into left lane and the Portola Plaza will be to your right.

*From North on Highway 1:*

Take the Del Monte/Pacific Grove exit, at seventh light, get into the left lane, and drive until you get to the Portola Plaza which will be to your right.

*From South/Carmel on Highway 1:*

Take the Aguajito exit, turn left at the first light (going under the freeway), follow Aguajito to Del Monte, turn left onto Del Monte, at third light get into left lane and the Portola Plaza will be on your right.

## **ADDITIONAL INFORMATION**

### **Message Desk:**

A Symposium Message Desk will be in operation in the Registration area during registration hours from Sunday, October 24 at 5pm to Wednesday, October 27 at noon. Please advise callers who wish to reach you during the day to ask the hotel operator for the IEEE CSIC Symposium message desk. The Portola Plaza main telephone number is 831-649-4511. Please check the message board periodically during the Symposium.

### **Distribution of Relevant Information:**

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to indiscriminately proliferate the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition.

### **Meeting Room Locations:**

#### **No Photographic and/or Recording Equipment:**

No photographic or recording equipment will be permitted at any time during the technical sessions of the IEEE CSIC Symposium.

### **Breakfasts:**

On Sunday, October 24, a continental breakfast will be available for Short Course registrants only in the Lower Atrium. There will be a complimentary continental breakfast for all Symposium attendees to be held in the De Anza Foyer on Monday, Tuesday and Wednesday.

### **Coffee Breaks:**

The locations of coffee breaks will be as follows:

Short Course Registrants (only) –  
Sunday, October 24: Lower Atrium

Primer Course Registrants (only) –  
Sunday, October 24: Lower Atrium

Symposium Registrants –  
Monday, October 25: De Anza Foyer  
Tuesday, October 26: De Anza Foyer  
Wednesday, October 27: Serra Ballroom

### **Symposium Social Events:**

#### **SYMPOSIUM OPENING RECEPTION.**

We welcome you to Monterey on Sunday evening, October 24th from 5:30 p.m. to 8:30 p.m. in the De Anza I and Foyer of the Portola Plaza Hotel Monterey. Come and meet up with your old friends and make new acquaintances over light hors d'oeuvres and wine, beer, or soft drinks. One free admission is included with your registration including two drink tickets, and extra tickets may be purchased at registration for \$30.

### EXHIBITION OPENING RECEPTION

Our exhibitors are hosting a reception to mark the exhibition opening on Tuesday, October 26 from 5:00 p.m. to 7:00 p.m. Every Symposium participant is invited to enjoy the hors d'oeuvres and schmooze and cruise the exhibits in the Serra Ballroom of the Monterey Conference Center adjacent to the Portola Plaza Hotel.

### EXHIBITION LUNCH

On Wednesday at noon, the Exhibition Luncheon will be hosted in the Serra Ballroom of the Monterey Conference Center adjacent to the Portola Plaza Hotel. The lunch is free to all Symposium participants, so come along, visit with the exhibitors, ask questions, make deals and find out what is going on in our industry.

### SYMPOSIUM PARTY

Join us for the Symposium Theme Party on Monday, October 25, from 7:00pm to 10:00pm in the De Anza III Room in the Portola Plaza Hotel. This year's Symposium Theme Party is a Multifunctional Integrated Event featuring a Casino Nite by The Entertainment Team, Inc. – a Northern California's Premier, The Monterey International Music Team – a Kelly Production's, and an excellent Monterey Fisherman's Wharf dinner buffet displaying the tradition of Monterey's Old Fisherman's Wharf, beer, wine, and soft drinks.

The Casino Nite package includes blackjack, craps, roulette, and paigow machines/tables with dealers to entertain more than 200 players at a time. The Monterey International Trio's blend of well-loved songs from around the world including Italian, French, Gypsy, Latin, German, Viennese, and American Jazz Standards will be also a unique experience. Whether they play your favorite musicals, tangos, swing tunes or waltzes, you'll find yourself tapping your foot during your Casino Nite with your glass of drink in one hand and throwing your dice for the roulette by the other hand, after an excellent seafood dinner.

This fascinating atmosphere and the good food and refreshments will provide an excellent time to meet with colleagues old and new. One free admission to the Symposium Party is included with each full registration, and extra tickets can be purchased at the registration center for only \$75.

## **Monterey Attractions:**

Among the many features Monterey itself has to offer is historic Cannery Row, a popular visitor area offering a multitude of unique galleries, shops, wine tasting rooms, and restaurants. Fisherman's Wharf, once the center of Monterey's fishing industry, also offers seafood restaurants, fish markets, and specialty shops. Sight-seeing and whale-watching charter and tour companies operate off the wharf daily. Within driving distance of the Monterey are numerous wineries offering tours, as well as opportunities for scenic hiking, biking, water sports, golf, and even rock climbing.

## **Weather:**

There is a significant variance in temperatures and weather patterns throughout Monterey County. The average maximum for October in the Monterey Peninsula is 70.4F and the average minimum 50.8F. It is advisable to dress in layers, with light to medium weight clothes during

the day, and sweaters and jackets at night. For weather information, call 831-656-1725.

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## **SYMPOSIUM HIGHLIGHTS**

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### **Technical Program:**

The technical program for the 2004 IEEE CSIC Symposium consists of over 64 technical papers, five panel sessions, an Industry Exhibit, and two Short Courses, "Power Amplifier Technologies and Markets for Compound Semiconductors" and "High Speed Data Converters." We will also be offering our annual introductory level class "Basics of Compound Semiconductor ICs" (Primer Course). This year we have invited 22 papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, we will continue the tradition of including important "late breaking news" papers.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. There is a tremendous amount of activity in the wireless and optical communication areas, as well as a strong interest in military electronics.

### **Short Course 1: "Power Amplifier Technologies and Markets for Compound Semiconductors"**

#### Short Course Description

One of the few undisputed domains for compound semiconductors is the power amplifier. This short course will present the current production state of the art for several power amplifier markets. Markets covered include basestation, handset, wireless LAN and mmW power amplifiers.

Each presentation will follow a similar structure including a description of the market characteristics, specifications specific to the application, technology considerations, design considerations and finally a circuit design example.

#### Topics Covered and Instructors:

Base Station PAs - John Gajadharsing

Handset PAs - Dr. Gene Tkachenko

Wireless LAN PAs - Michael Sagebiel

mmW PAs - Mansoor Siddiqui

Linearization Techniques - Markus Mayer

### **Short Course 2: "High Speed Data Converters"**

#### Short Course Description

High speed converters are moving up in frequency and allowing the digital domain to take over more and more of what were analog functions. This course will provide an overview of high speed converters including technology considerations, circuit topologies and applications.

#### Topics Covered and Instructors:

Technology for ADC Circuits - M. Frank Chang

Delta Sigma Converters - Martin Snelgrove  
High Speed Track and Hold Circuits - M.J. Choe  
Baseband High Speed Low Resolution Converters - Jaesik Lee  
The ADC Story for Wireless Consumer Platforms - Raf Roovers

In the unlikely event that an instructor is unable to participate, an alternate instructor may be substituted.

Registration for the course is as noted in "Registration". A limited number of Short Course Notes will be available after the course for purchase by Symposium registrants, subject to availability.

Direct questions to:  
Mitch Shifrin, Short Course Organizer  
Hittite Microwave  
978-250-3343  
mits@hittite.com

### **Primer Course: Basics of Compound Semiconductor ICs**

The CSIC Symposium will again offer an introductory-level class, "Basics of GaAs, InP, and SiGe RFICs," intended for professionals in the electronics industry with little or no experience in compound semiconductor ICs or for anyone who wants an excellent review. The class covers analog/microwave and optical communications ICs and their applications. The material is designed to provide a brief overview of concepts and issues unique to compound semiconductor ICs so that participants will be better able to profit from the Symposium Technical Program. The class is taught by Donald B. Estreich, an Agilent Technologies manager with 24 years experience in design and application of GaAs analog and microwave ICs, and Stephen Long, a University of California, Santa Barbara professor, also with 24 years experience in GaAs IC development. The class will be held Sunday evening, October 24<sup>th</sup>, from 4:00 p.m. to 7:00 p.m.

The registration fee is \$175 for professionals and \$75 for students. The fee includes a handout containing a copy of the overheads with an extensive reference list. Space is limited, so **ADVANCE REGISTRATION IS HIGHLY RECOMMENDED**. For additional information, please contact the Primer Course Coordinator:

William Peatman  
ANADIGICS, Inc.  
Warren, NJ  
(908) 668-5000 x5842

Registration for the class is as noted in "Registration". A limited number of copies of the handouts will be available to symposium registrants, subject to availability. The cost is \$50.

### **Panel Sessions:**

This year we have five exciting Panel Sessions spread over the 3 days of the technical sessions. These are intended to be timely, thought-provoking, educational, and possibly even controversial. **This year we will have a joint panel with CS-MAX on semiconductor foundries. Free attendance will be honored for CS-MAX conference registrants. The 5 panel topics are as follows:**

Panel Session 1:  
**“What technology gives the ultimate high-speed data converter.  
CMOS, SiGe, III-V HBT?”**  
Monday, October 25<sup>th</sup>; 3:40-5:10 p.m.

Panel Session 2:  
**“Integrated PA Module Packaging Shoot-Out”**  
Monday, October 25<sup>th</sup>; 3:40-5:10 p.m.

**Panel Session 3 – Joint with CSMAX:**  
**“III-V Foundries Pure-play vs Captive”**  
Tuesday, October 26<sup>th</sup>; 1:20p.m. – 3:10 p.m.

Panel Session 4:  
**“When will 40G Market Materialize?”**  
Wednesday, October 27<sup>th</sup>; 1:00 p.m. – 2:30 p.m

Panel Session 5:  
**“mmW Technology Free For All”**  
Wednesday, October 27<sup>th</sup>; 1:00 p.m. – 2:30 p.m

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to their day and time).

## **Compound Semiconductor Week 2004 Technology Exhibition:**

The 2004 CS-Week Technology Exhibition will be held concurrently with both the IEEE CSIC Symposium and CSMAX on October 26<sup>th</sup> and 27<sup>th</sup> in the Serra Ballroom located in the Monterey Conference Center. The Exhibition is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, related services, commercial and military applications. The early list of exhibitors already includes:

Accent Optical Technologies  
Aixtron  
AXIC, Inc.  
AXT, Inc.  
BOC Edwards  
Bruker AXS, Inc.  
Candela Instruments  
Compound Semiconductor Magazine  
CVD Equipment Corporation  
Dockweiler Ag  
Dow Corning Corporation  
Emcore Corporation  
Engis Corporation  
Freiberger USA  
GE Advanced Materials / Quartz  
GEO Gallium  
Implant Sciences Corporation  
INFICON  
Insaco, Inc.  
Intelligent Epitaxy Technology, Inc.  
J P Sercel Associates, Inc.  
Kopin Corporation, Inc.  
Marubeni America Corporation  
Matheson Tri-Gas  
MBE Technology Pte Ltd  
Modular Process Technology  
Nikko Materials  
Nippon Sanso Corporation  
Optical Metrology Innovations, Ltd.  
Oxford Instruments Plasma Technology  
Picogiga USA, Inc.  
Presidio Components, Inc.  
Qspec Technology  
Riber, Inc.  
Rohm And Haas Electronic Materials  
SAES Pure Gas, Inc.  
Saint-Gobain Abrasives  
Saint-Gobain Crystals  
Silvaco International  
Sumika Electronic Materials, Inc.  
Sumitomo Electric  
Thomas Swan  
Trion Technology  
Veeco Instruments  
Williams Advanced Materials  
Xpert Semiconductor, Inc.  
Zeland Software, Inc.

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 5:00 p.m. and 8:00 p.m. on Tuesday, October 26<sup>th</sup> and 7:30 a.m. to 4:00 p.m. on Wednesday, October 27<sup>th</sup>. The Exhibition will also host the Exhibition Opening Reception on Tuesday evening from 5:00 p.m. until 7:00 p.m. and the Exhibition Luncheon from 11:40 a.m. until 1:00 p.m. on Wednesday. All Symposium coffee breaks on Wednesday will be held in the exhibition area.

There is still time for additional organizations to participate in the Exhibition. Interested parties should contact Mr. Harry Kuemmerle of VIP Meetings & Conventions, Pacific Palisades, CA at (310) 459-4691, Fax (310) 459-0605, e-mail: [harry.k@vipmeetings.com](mailto:harry.k@vipmeetings.com). Or visit the VIP Meetings & Conventions website at [www.vipmeetings/conferences/csweek2004.html](http://www.vipmeetings/conferences/csweek2004.html) and click on **exhibition** to download application forms or for additional information on the Exhibition, including the latest list of exhibitors.

### **Late-Breaking News Papers:**

We have solicited papers containing late-breaking news for the Symposium Program. The times and locations of these presentations will be posted at the Symposium, as well as on the CSIC Symposium website at

<http://www.csics.org/>.

In addition, extended abstracts for these papers will appear in the Symposium Digest.

Late news paper submissions are due July 28 5PM EDT. Submissions must be submitted in 4 page extended abstract format and camera ready for digest printing. E-mail abstracts to [2004abstract@sirenta.com](mailto:2004abstract@sirenta.com)

### **Technical Digest:**

Extra copies of the Technical Digest can be purchased by Symposium registrants through Advance Registration. A limited number of digests will also be available for sale at the Registration Desk after 1:00 p.m. on Tuesday, October 26<sup>th</sup>. The cost of the paper bound digest, if ordered through Advance Registration or purchased on-site, is \$75. The CD ROM Digest for 2004 will also be offered for \$100. Both current and past digests will be available through IEEE after the Symposium by mail from the IEEE Customer Service Center, 445 Hoes Lane, Piscataway, NJ 08854 at (800) 701-4333.

### **Outstanding Paper Award:**

The 2004 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the Session Chairpersons. The award winner will be publicly announced shortly after this year's Symposium with the award formally presented at next year's Compound Semiconductor IC Symposium.

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## **Short Courses**

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**Sunday, October 24, 2004**  
**Portola Plaza Hotel at Monterey Bay**  
**Portola and Redwood Rooms**  
**8:30 a.m. - 3:30 p.m.**

**Course Coordinator:** Mitchell Shifrin  
Hittite Microwave  
978-250-3343  
mitschs@hittite.com

This year the CSIC Symposium will hold two short courses covering power amplifiers and high speed digital circuits.

### **“Power Amplifier Technologies and Markets for Compound Semiconductors” (Portola Room)**

#### **Short Course Description**

One of the few undisputed domains for compound semiconductors is the power amplifier. This short course will present the current production state of the art for several power amplifier markets. Markets covered include basestation, handset, wireless LAN and mmW power amplifiers.

Each presentation will follow a similar structure including a description of the market characteristics, specifications specific to the application, technology considerations, design considerations and finally a circuit design example.

#### **Topics Covered and Instructors:**

- a) Base Station PAs - John Gajadharsing
- b) Handset PAs - Dr. Gene Tkachenko
- c) Wireless LAN PAs - Michael Sagebiel
- d) mmW PAs - Mansoor Siddiqui
- e) Linearization Techniques - Markus Mayer

In the unlikely event that an instructor is unable to participate, an alternate instructor may be substituted.

## **Power Amplifier Short Course Schedule**

The course will be held on Sunday October 24th and will begin with a continental breakfast. Instructors will begin promptly at 8:30AM. A lunch will be provided as well a morning refreshment break.

- 7:30AM **Registration and Breakfast**  
(Portola Lobby and Lower Atrium)
- 8:30AM **Introduction and Overview (Portola Room)**  
Mitchell Shifrin, Hittite Microwave Corporation
- 8:35AM **Base Station PAs**  
John Gajadharsing, Philips research
- 9:35AM **Handset PAs**  
Dr. Gene Tkachenko, Skyworks Solutions, Inc
- 10:35AM **Coffee Break**
- 10:50AM **Wireless LAN PAs**  
Michael Sagebiel, Atmel
- 11:50PM **Lunch (Lower Atrium)**
- 1:10PM **mmW PAs**  
Mansoor Siddiqui, TRW
- 2:10PM **Linearization Techniques**  
Markus Mayer, Vienna University of Technology,  
Institute for Electrical Measurements and Circuit  
Design
- 3:10PM **Questions and Discussion**
- 3:30PM **Close of Short Course**

## **“High Speed Data Converters” (Redwood Room)**

### **Short Course Description**

High speed converters are moving up in frequency and allowing the digital domain to take over more and more of what were analog functions. This course will provide an overview of high speed converters including technology considerations, circuit topologies and applications.

Topics Covered and Instructors:

- a) Technology for ADC Circuits - M. Frank Chang
- b) Delta Sigma Converters - Martin Snelgrove
- c) High Speed Track and Hold Circuits - M.J. Choe
- d) Baseband High Speed Low Resolution Converters - Jaesik Lee
- e) The ADC Story for Wireless Consumer Platforms - Raf Roovers

In the unlikely event that an instructor is unable to participate, an alternate instructor may be substituted.

## Converter Short Course Schedule

The course will be held on Sunday October 24th and will begin with a continental breakfast. Instructors will begin promptly at 8:30AM. A lunch will be provided as well as a morning refreshment break.

- 7:30AM **Registration and Breakfast**  
(Portola Lobby and Redwood Room)
- 8:30AM **Introduction and Overview (Redwood Room)**  
Mitchell Shifrin, Hittite Microwave Corporation
- 8:35AM **Technology for ADC Circuits**  
M. Frank Chang, UCLA
- 9:35AM **Delta Sigma Converters**  
Martin Snelgrove, Dissonance
- 10:35AM **Coffee Break**
- 10:50AM **High Speed Track and Hold Circuits**  
M.J. Choe., Rockwell Scientific LLC.
- 11:50PM **Lunch (Lower Atrium)**
- 1:10PM **Baseband High Speed Low Res Converters**  
Jaesik Lee, Lucent
- 2:10PM **ADCs for Wireless Consumer Platforms**  
Raf Roovers, Philips research
- 3:10PM **Questions and Discussion**
- 3:30PM **Close of Short Course**

## Who Should Attend

The short courses are a must for everyone interested in knowing the latest in advanced design technologies and their applications to both defense and commercial markets. Our lectures will cater to a range of interests and experience levels. The course is designed to give all attendees a solid overview of the device technology from device physics fundamentals through specific circuit examples and applications.

## Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for the Short Courses. A limited number of registrations will be available on-site immediately prior to the start of the course. The price for the Short Course is \$350 for those that pre-register, and \$450 for those that register on-site. The price for students is \$200 for those that pre-register, and \$300 for on-site registration. The registration fee includes the lectures, a book of Short Course Notes, continental breakfast, lunch, and morning/afternoon refreshments. Additional copies of the Short Course Notes may be purchased for \$100 each.

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# Primer Course

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**Sunday, October 24, 2004**  
**Portola Plaza Hotel**  
**(Portola Room)**  
**4:00 p.m. - 7:00 p.m.**

## "Basics of Compound Semiconductor ICs"

**Instructors:**                      **Stephen I. Long**  
University of California  
Santa Barbara, CA  
**Donald B. Estreich**  
Agilent Technologies  
Santa Rosa, CA

**Course Coordinator:**          **William Peatman**  
ANADIGICS, Inc.

### Course Objective and Description:

The popular primer course "Basics of Compound Semiconductor ICs" is an introductory-level class intended for professionals in the electronic industry with little or no experience in compound semiconductor IC technology. It also provides an excellent review for those with more experience. The course covers: digital and analog/RF/microwave circuits; III/V materials including wide bandgap GaN and SiC; MOS and bipolar devices; and fabrication technology. The course is tailored to provide background for symposium participants to better understand and appreciate the papers presented, including a glossary of those ever-cryptic acronyms. Throughout the course, comparisons among the GaAs technologies will be presented as well as comparisons with silicon technologies. Also, a number of GaAs integrated circuits along with the intended applications will be described.

Instructors Stephen I. Long and Donald B. Estreich each have over 25 years of experience working with GaAs ICs. A copy of their viewgraphs with an extensive bibliography will be distributed to each Primer Course registrant. Ample discussion time will provide an opportunity for participants to have questions answered by the instructors.

### Course Agenda:

4:00 p.m. Introduction  
4:05 p.m. GaAs History, Materials, and Processes  
4:30 p.m. Device Operation  
5:00 p.m. Discussion  
5:10 p.m. Break  
5:20 p.m. Digital Circuits  
6:00 p.m. Analog/RF/Microwave Circuits  
6:40 p.m. Summary and Discussion  
7:00 p.m. Close

## **OTHER MEETINGS**

### **2004 Reliability of Compound Semiconductors [ROCS] Workshop: (formerly GaAs Reliability Workshop) (De Anza III) 8:00 a.m. - 5:00 p.m.**

The 19th annual ROCS Workshop - formerly known as the GaAs Reliability Workshop - will be held in conjunction with CSICS on Sunday October 24, 2004, at the Portola Plaza Hotel in Monterey, CA. This meeting is sponsored by the JEDEC JC-14.7 Committee on GaAs Reliability and Quality Standards and the EIA, and with co-sponsorship of the Electron Devices Society of the IEEE.

The ROCS Workshop brings together researchers, manufacturers and users of compound semiconductor materials, devices and circuits. Papers presenting latest results, including work-in-progress and new developments in all aspects of compound semiconductor reliability will be presented. Potential authors are invited to submit an electronic copy of a one to two page comprehensive summary, suitable for a 15 minute presentation, to: Peter Ersland, [erslandp@tycoelectronics.com](mailto:erslandp@tycoelectronics.com) (978) 656-2817. The deadline for receipt of submissions is August 16, 2004, and late papers of significant interest will be considered up to the Workshop. The Advanced Program will be published at <http://www.jedec.org/Home/gaas/default.cfm> approximately one month prior to the meeting.

Registration for the workshop is \$125.00 in advance, or \$175.00 at the door. To pre-register, mail your name, Post Office address, email address, and phone number with a check for \$125 to: EIA/JEDEC, JC-14.7 Workshop, 2500 Wilson Boulevard, Arlington, VA 22201-3834 by October 11, 2004. Visa, MasterCard and American Express credit cards are also accepted. Registration includes a full day of ROCS presentations, two breaks, a luncheon and a copy of the Proceedings. Late registration will be available from 7:30 a.m. to 8:00 a.m. on the morning of the workshop. For further information or to download a pre-registration form, visit our WEB site at [www.jedec.org](http://www.jedec.org) and click on GaAs, or contact: Dr. Anthony A. Immorlica, Jr., Workshop Chairman, BAE SYSTEMS, P.O. Box 868, MER15-1351, Nashua, NH 03061-0868, (603) 885-1100, [anthony.a.immorlica@baesystems.com](mailto:anthony.a.immorlica@baesystems.com).

## **SEMI Compound Semiconductor Materials and ASTM Committee Meeting**

The next SEMI Standards Compound Semiconductor Materials Committee meeting is scheduled during the IEEE CSIC Symposium for Tuesday, October 26, 2004 from 8:00-10:00 PM (PST) in Redwood I Meeting Room at the Portola Plaza Hotel in Monterey, California.

SEMI and ASTM hold joint meetings to develop test methods and specifications as a cooperative effort.

The SEMI Standards Compound Semiconductor Materials Committee cordially invites the 2004 IEEE CSIC Symposium attendees interested in the development of internationally approved standards for Wafer Specifications (GaAs, InP, SiC dimensions/orientation, electrical properties), Epitaxy Layer Specifications, non-destructive mobility measurements, eddy current probe measurement resolution, test methods for etch pit density (EPD), room temperature resistivity mapping and investigations of electronic data interchange (EDI) codes for wafer marking to attend the next standards meeting on October 26, 2004.

SEMI is a global industry association for companies participating in the microelectronics and display industries. SEMI maintains offices in Austin, Beijing, Brussels, Hsinchu, Moscow, San Jose (Calif.), Seoul, Singapore, Tokyo, Shanghai and Washington, D.C. For more information, visit SEMI at [www.semi.org](http://www.semi.org).

For additional information, please contact:

**Committee Co-chair:**

James Oliver  
Northrop-Grumman  
P.O. Box 1521 M/S 3K13  
Baltimore, MD 21203  
Phone: 410-765-0117  
[j.oliver@ngc.com](mailto:j.oliver@ngc.com)

**Committee Co-chair:**

Russ Kremer  
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10151 Stroud Lane  
Dayton, OH 45458  
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# SYMPOSIUM PROGRAM

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**Monday, October 25, 2004**

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## **REGISTRATION AND CONTINENTAL BREAKFAST**

7:00 a.m. - 5:00 p.m.

**Registration – Portola Lobby**

7:00 a.m. - 8:00 a.m.

**Continental Breakfast - De Anza Foyer**

## **SYMPOSIUM OPENING**

8:00 a.m. - 8:25 a.m.

**De Anza I&II – Portola Plaza**

**Introduction and Awards Presentation**

**2004 Symposium Chairman**

Brad Nelson, *Sirenza Microdevices*

**2004 Technical Program Chairman**

Kevin Kobayashi, *Sirenza Microdevices*

## **SESSION A: PLENARY SESSION**

8:30 a.m. – 12:00 p.m.

**De Anza I&II – Portola Plaza**

**Chairpersons:** Mitch Shifrin, *Hittite*  
Joy Laskar, *Georgia Tech University*

8:30 a.m.

**A.1 Wireless Basestation Technology Evolution**

Bill Vassilakis, *Powerwave Technologies Inc*, Santa Ana, CA

9:00 a.m.

**A.2 3D Microsystems as the Next Revolution to**

**Enable System Level Integration and Scaling**

Zachary J. Lemnios, *DARPA/MTO*, Arlington VA

9:30 a.m. - 10:00 a.m. **Coffee Break**

10:00 a.m.

**A.3 Venture Investing in Semiconductors**

Arati Prabhakar, *US Venture Partners*

10:30 a.m.

**A.4 Advances in SiGe HBT Technology in Europe**

H. Rücker and W. Winkler, *IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*

11:00 a.m.

**A.5 Recent Progress and Future Prospects for GaN HEMTs in Base-Station Applications**

Toshihide Kikkawa, *Fujitsu Laboratories Ltd.*, 10-1 Morinosato-Wakamiya, Atsugi, Kanagawa, 243-0197, Japan

11:30 a.m.

**A.6 Opening the Terahertz Window**

Thomas Crowe, *Dept. of Electrical Engineering, University of Virginia, Virginia Diodes, Inc.*, Charlottesville, VA 22903

12:00 noon **End of Session A**

12:00 noon - 1:20 p.m. **Break for Lunch**

**Monday, October 25, 2004**

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**SESSION B: Mixed Signal Circuits and Technology**

1:20 p.m. – 3:10 p.m.

**De Anza I - Portola Plaza**

**Chairpersons:** Bill Skones, *NGST*  
Todd Kaplan, *HRL*

1:20 p.m.

**B.1 Architectures for High-Speed Data Converters (Invited)**  
Martin Snelgrove, *Consultant*

1:50 p.m.

**B.2 Semiconductor Technology Considerations in High-Speed Data Conversion (Invited)**  
M. Frank Chang, *Electrical Engineering Department, University of California at Los Angeles, Los Angeles, CA*

2:20 p.m.

**B.3 SiGe BiCMOS Technologies - Addressing the Communication Market Needs (Invited)**  
Alvin J. Joseph, *Semiconductor Research and Development Center, IBM Microelectronics Division, Essex Junction, Vermont 05452*

2:50 p.m.

**B.4 Full Nyquist 4-bit ADC Operating at Half Clock Rate in InP-HBT Technology**  
Charles Kaplan and Douglas McLaughlin, *HRL-Laboratories LLC, 3011 Malibu Canyon Road, Malibu, CA. 90265*

3:10 p.m.

**End of Session B**

3:10 p.m. - 3:40 p.m. **Coffee Break**

**SESSION C: High Power Amplifiers Below 5GHz**

1:20 p.m. – 3:10 p.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Freek van Straten, *Philips Semiconductors*  
Dave Halchin, *RF Micro Devices*

1:20 p.m.

**C.1 A Novel Compact Composite Power Cell for High Linearity Power Amplifiers in InGaP HBTs**  
H. Gao, H. Zhang, H. Guan, Li-Wu Yang\* and G. P. Li, *University of California Irvine, RF Integrated Corporation\*, Engineering Gateway West Wing 3321, UC Irvine, 92697*

1:40 p.m.

**C.2 Design and Development of Compact CDMA/WCDMA Power Amplifier Module for High Yield Low Cost Manufacturing**  
S. Xu, R. Frey, M. Anderson, T. Chen, A. Prejs, J. Miller, R. Abromovich, T. Arell, M. Singh, R. Schrock, A. Parish, E. Demarest and J. Ryan, *Anadigics, Inc., Warren, New Jersey, 07059, USA*

**Monday, October 25, 2004**

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2:00 p.m.

**C.3 High Efficiency CDMA Power Amplifier with Dynamic Current Control Circuits**

Y. Yang, *Skyworks Solutions Inc., Newbury Park, CA 91320, USA*

2:20 p.m.

**C.4 C-band GaAs FET Power Amplifiers with 70-W Output Power and 50% PAE for Satellite Communication Use**

A. Wakejima \*, T. Asano \*\*, T. Hirano \*\*, M. Funabashi \*\*, and K. Matsunaga \*, \**System Devices Research Laboratories, NEC Corporation, 2-9-1 Seiran, Otsu, Shiga 520-0833, Japan;* \*\**NEC TOSHIBA Space Systems, Ltd., Tsuzuki-ku, Yokohama, 224-8555, Japan.*

2:40 p.m.

**End of Session C**

3:10 p.m. - 3:40 p.m. **Coffee Break**

**PANEL SESSION 1:**

**What technology gives the ultimate high-speed data converter. CMOS, SiGe, III-V HBT?**

3:40 p.m.-5:10 p.m.

**De Anza II – Portola Plaza**

**Moderators:** Todd Kaplan, *HRL Laboratories, LLC*  
William Skones, *Northrup Grumman*

High-speed data converter design has long been dominated by the bipolar transistor, with silicon and III/V technologies competing for the speed title. Will advances in InP HBT technology allow it to at last fulfill its promise to dominate, or will advances in SiGe technology enable silicon to retain its advantage? Meanwhile, CMOS looms in the background. The panelists will provide their unique perspectives and field your questions on the current state-of-the-art, and the future of high-speed ADC and DAC technology.

**Panel Members:**

Frank Chang	<i>UCLA</i>
Mark Englekirk	<i>Peregrine Semiconductor</i>
Jaesik Lee	<i>Lucent Technologies</i>
Bert Oyama	<i>Northrop Grumman Space Technology</i>
Martin Snelgrove	<i>Consultant</i>
TBD	<i>DARPA MTO</i>

**Monday, October 25, 2004**

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**PANEL SESSION 2:  
Integrated PA Module Packaging Shoot-Out**

3:40 p.m. - 5:10 p.m.

**De Anza I – Portola Plaza**

**Moderators:** Julio Costa, *RF Micro Devices*  
William Peatman, *ANADIGICS*

The Power Amplifier Module package and assembly is one of the most critical and “make or break” process steps in the PA manufacturing sequence. Different module techniques are currently being used. How do you make the choice between laminate, lead-frame or ceramic if you are a small vs. large PA supplier? This panel will cover packaging technology and trends. Package techniques to be debated include

Multi-Layer Laminate – Running out of Gas?

Lead-Frame – Just Flash in the Pan?

LTCC – Does Cost and Cycle-Time Fit the Business Model?

The panelists will present their best cases for each technology and indicate what developments they plan for successive generations. Issues including cost, design complexity, cycle times, integration limits, quality issues and future requirements will help distinguish the competing technologies.

**Panel Members:**

Mike Anderson	<i>ANADIGICS</i>
Christian Block	<i>EPCOS</i>
Albert Gu	<i>Sawtek/TriQuint</i>
Marnie Mattei	<i>RF Micro Devices</i>
Christopher Scanlan	<i>AMKOR</i>
Cliff Vaughn	<i>Motorola</i>

Monday, October 25, 2004

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*Symposium Theme Party*

*Casino Nite*

*De Anza III*

*7:00 p.m. - 10:00 p.m.*

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**Tuesday, October 26, 2004**

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**REGISTRATION AND CONTINENTAL BREAKFAST**

7:00 a.m.- 5:00 p.m.

**Registration – Portola Lobby**

7:30 a.m. - 8:30 a.m.

**Continental Breakfast – De Anza Foyer**

**SESSION D: HBTs**

8:00 a.m. – 9:50 a.m.

**De Anza I – Portola Plaza**

**Chairpersons:** Cedric Monier, *NGST*  
Greg U'Ren, *Jazz Semiconductor*

8:00 a.m.

**D.1 High Reliability High Voltage HBTs Operating up to 30 V (Invited)**

Tim Henderson and John Hitt, *TriQuint Semiconductor Texas, Richardson, TX 75080*

8:30 a.m.

**D.2 Defect analysis of degraded InGaP/GaAs HBTs**

R. Pazirandeh<sup>1</sup>, U. Zeimer<sup>1</sup>, H. Kirmse<sup>1</sup>, J. Würfl<sup>2</sup>, G. Tränkle<sup>2</sup>, W. Österle<sup>2</sup>, *Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany*, <sup>1</sup>*Humboldt Universität zu Berlin, Institut für Physik, Kristallographie, Berlin, Germany*, <sup>2</sup>*Bundesanstalt für Materialforschung und -prüfung, Berlin, Germany*

8:50 a.m.

**D.3 Experimental Probe of the Minority Carrier Velocity Profile Across GaAs HBT Base Layers**

E.M. Rehder\*, C.R. Lutz\*, and R.E. Welsler\*, P. J. Zampardi, *\*Kopin Corp, Taunton, MA, Skyworks Solutions, Newbury Park, CA*

9:10 a.m.

**D.4 State of the art thermal analysis of GaAs/InGaP HBT**

PJ van der Wel<sup>1</sup>, J. Bielen<sup>1</sup>, T. Henderson<sup>2</sup>, J. Middleton<sup>3</sup>, <sup>1</sup>*Philips Semiconductors, Nijmegen, The Netherlands*, <sup>2</sup>*TriQuint Semiconductor, Dallas, TX*, <sup>3</sup>*TriQuint Semiconductor, Hillsboro, OR*

9:30 a.m.

**End of Session D**

9:50 a.m. – 10:20 a.m. **Coffee Break**

**SESSION E: Optical System Building Blocks**

8:00 a.m. – 9:50 a.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Anu Mahajan, *TriQuint Semiconductor*  
Kenjiro Nishikawa, *NTT*

8:00 a.m.

**E.1 Photoreceiver architectures beyond 40 Gbit/s (Invited)**

Hiroshi Ito, *NTT Photonics Laboratories, NTT Corporation, Atsugi-shi, Kanagawa 243-0198, Japan*

**Tuesday, October 26, 2004**

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8:30 a.m.

**E.2 InP DHBT Mixed-Signal Specific ICs for Advanced 40 Gb/s Transmitters**

J. Godin, A. Konczykowska, M. Riet, P. Berdaguer, J. Moulu, V. Puyal, F. Jorge, S. Vuye, R. Lefèvre, *ALCATEL R&I / OPTO+*,  
*Route de Nozay, 91460 Marcoussis, France*

8:50 a.m.

**E.3 Paper Withdrawn: Digital SiGe-Chips for data transmission up to 86 Gbit/s**

O. Wohlgenuth, W. Müller, P. Paschke, T. Link, R. Lederer, B. Kolb, H. Dotzauer, *Lucent Technologies, 90411 Nuremberg, Germany*

8:50 a.m.

**E.3L Late News Paper: A 2-Bit 20 Gbps InP HBT A/D Converter for Optical Communications**

Zheng Guo, Matt D'Amore, Augusto Gutierrez, *Northrop Grumman Space and Technology, Redondo Beach, CA, USA*

9:05 a.m.

**E.4L Late News Paper: A Fast Low-Power 4x4 Switch IC Using InP HEMTs for 10-Gbit/s Systems**

Hideki Kamitsuna, Yasuro Yamane, Masami Tokumitsu, Hirohiko Sugahara, and Masahiro Muraguchi, *NTT Photonics Laboratories, NTT Corporation, Kanagawa, Japan*

9:20 a.m.

**E.5L Late News Paper: A 49-Gb/s, 7-Tap Transversal Filter in 0.18µm SiGe BiCMOS for Backplane Equalization**

Altan Hazneci and Sorin P. Voinigescu, *Department of Electrical & Computer Engineering, University of Toronto, Toronto, Ontario, Canada*

9:35 a.m.

**E.6L Late News Paper: A 60-Gb/s 0.7-V 10-mW Monolithic Transformer-Coupled 2:1 Multiplexer in 90 nm CMOS**

Daniel Kehrer, Hans-Dieter Wohlmuth, *INFINEON Technologies AG, Corporate Research, Munich, Germany*

9:50 a.m.

**End of Session E**

9:50 a.m. – 10:20 a.m. **Coffee Break**

**Tuesday, October 26, 2004**

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**SESSION F: FETs**

10:20 a.m. – 12:10 p.m.

**De Anza I – Portola Plaza**

**Chairpersons:** John Martinez, *BAE Systems*  
Marc Rocchi, *OMMIC*

10:20 a.m.

**F.1 High Yield Enhancement and Depletion-Mode pHEMT  
Using 6 inch GaAs Production Process**

Y. Y. Hsieh, H.C.Chiu, T.J. Yeh, C.G.Yuan, T. Hwang, P. Yeh,  
J. H. Hwang, C.S.Wu, *WIN Semiconductors Corp, Taiwan,*  
*R.O.C*

10:40 a.m.

**F.2 A Robust and Manufactureable E-/D-mode pHEMT  
Production Process Utilizing Multi-Level, Low-Dielectric  
Constant, High Density Interconnects on 150mm Substrates**  
W. A. Wohlmut, W. Liebl, O. Berger, *TriQuint Semiconductor,*  
*Hillsboro, OR 97124, \*TriQuint Semiconductor, Nashua, NH*  
*03061*

11:00 a.m.

**F.3 Low Insertion Loss Switch Technology Using 6-inch  
InGaP/InGaAs pHEMT Production Process**

H.C.Chiu, T.J. Yeh, Y.Y.Hsieh, C.G.Yuan, Y.C.Wang, T.  
Hwang, P. Yeh, C.S.Wu, *WIN Semiconductors Corp, Taiwan,*  
*R.O.C*

11:20 a.m.

**F.4 Reliability Consideration of GaAs PHEMT Schottky Diodes  
for Mixer Applications**

Y.C. Chou, D. Leung, M. Biedenbender, O Fordham, R.  
Grundbacher, Q. Kan, P.H. Liu, D. Eng, R. Lai, T. Block, and A.  
Oki, *Northrop Grumman Space Technology, Redondo Beach,*  
*CA*

11:40 p.m.

**End of Session F**

12:10 p.m. - 1:20 p.m. **Break for Lunch**

**SESSION G: High Performance MMIC Power  
Amplifiers**

10:20 a.m. – 12:10 p.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Tony Quach, *Air Force Research Labs*  
Gary Valentine, *Raytheon Electronic Systems*

10:20 a.m.

**G.1 A Low Cost Power Amplifier for 5-GHz W-LAN  
Applications (invited)**

A. Scuderi<sup>1</sup>, F. Carrara<sup>2</sup> and G. Palmisano<sup>2</sup>  
<sup>1</sup>*STMicroelectronics, Catania, Italy,* <sup>2</sup>*Università di Catania,*  
*Facoltà di Ingegneria, DIEES, Catania, Italy.*

**Tuesday, October 26, 2004**

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10:50 a.m.

- G.2 **A High Power Q-Band MMIC Power Amplifier Based on Dual-Recess 0.15  $\mu$ m pHEMT**  
Q. H. Wang, M.Y. Yao, S. Nayak, K. Kong, C. F. Campbell,  
*TriQuint Semiconductor, Richardson, TX*

11:10 a.m.

- G.3 **A Fully Matched 8W X-band PHEMT MMIC High Power Amplifier**  
C. K. Chu, H. K. Huang, H. Z. Liu, R. J. Chiu, C. H. Lin, C. C. Wang and Y. H. Wang +; C. C. Hsu, W. Wu, C. L. Wu and C. S. Chang, *Institute of Microelectronics, Department of Electrical Engineering, National Cheng-Kung University, Tainan, 701 Taiwan, R.O.C.; Transcom, Inc. Tainan, 741 Taiwan, R.O.C.*

11:30 a.m.

- G.4 **Paper Withdrawn: A Highly Efficient Broadband (8-10 GHz) Monolithic Class E Power Amplifier**  
R. Tayrani, *Raytheon Space & Airborne Systems, El Segundo, CA 90245*

11:30 a.m.

- G.4L Late News Paper: **A 20 GHz Low Noise Amplifier with Active Balun in a 0.25  $\mu$ m SiGe BICMOS Technology**  
Brian Welch, Kevin Kornegay, Hyun-Min Park, Joy Laskar\*, *Cornell University, Ithaca New York, USA, \* Georgia Institute of Technology School of ECE, Atlanta, Georgia, USA*

11:45 p.m.

- G.5L Late News Paper: **A 90-GHz InP-HEMT Lossy Match Amplifier with 20-dB Gain Using a Broadband Matching Technique**  
Y. Inoue, M. Sato, Y. Kawano, S. Masuda, T. Ohki, K. Makiyama, K. Takahashi, H. Shigematsu, and T. Hirose, *Fujitsu Laboratories Ltd., Morinosato-Wakamiya, Atsugi, Japan*

12:00 noon

**End of Session G**

12.10 a.m. - 1:20 p.m. **Break for Lunch**

**Tuesday, October 26, 2004**

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**SESSION H: Novel Signal Generation and Switching ICs**

1:20 p.m. – 3:10 p.m.

**De Anza I – Portola Plaza**

**Chairpersons:** Mohammad Madihian, *NEC Labs. America, Inc.*  
Chul Soon Park, *Information and Communications University, Korea*

1:20 p.m.

**H.1 A 5 GHz Fully Integrated Full PMOS Low**

**Phase Noise LC VCO**

G. De ASTIS<sup>1</sup>, D. CORDEAU<sup>1,2</sup>, J.-M.

PAILLOT<sup>2</sup>, L. DASCALESCU<sup>2</sup>, <sup>1</sup>ACCO, *Saint-Germain-en-Laye, France*, <sup>2</sup>Laird-Esip, *Upres\_EA 1219, IUT d'Angoulême-4, Angoulême, France*

1:40 p.m.

**H.2 A x2 Coupled Colpitt VCO with Ultra Low Phase Noise**

H. Zirath, R. Kozuharov, M. Ferndahl, *Chalmers University of Technology, Göteborg, Sweden*

2:00 p.m.

**H.3 Fundamental Low Phase-Noise Monolithic InP-Based DHB T VCOs**

**With High Output Power Operating up to 75 GHz**

R.-E. Makon, K. Schneider, R. Driad, M. Lang, R. Aidam, R. Quay, and G. Weimann, *Fraunhofer Institute of Applied Solid-State Physics (IAF), D-79108 Freiburg, Freiburg, Germany*

2:20 p.m.

**H.4 A 1.9 GHz SPDT Switch Implemented with GaN HFETs Featuring Two Different Depth Depth-Recesses in i-AlGaN**

M. Hirose, Y. Takada, M. Kuraguchi, T. Sasaki, and K. Tsuda *Corporate R&D Center, Toshiba Corp., 1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan*

2:40 p.m.

**H.5L Late News Paper: A Low Power (45mW/latch) Static 150GHz CML Divider**

Donald A. Hitko, Tahir Hussain, Joseph F. Jensen, Yakov Royter, Susan L. Morton, David S. Matthews, Rajesh D. Rajavel, Ivan Milosavljevic, Charles H. Fields, Stephen Thomas III, Ara Kurdoghlian, Zhihao Lao, Kenneth Elliott, Marko Sokolich, *HRL Laboratories, LLC, Malibu, CA 90265 USA*

2:55 p.m.

**H.6L Late News Paper: 120-GHz Tx/Rx Chipset for 10-Gbit/s Wireless Applications Using 0.1- $\mu$ m-gate InP HEMTs**

Toshihiko Kosugi, Masami Tokumitsu, Takatomo Enoki, Masahiro Muraguchi, Akihiko Hirata\*, and Tadao Nagatsuma\*, *NTT Photonics Laboratories, NTT Corporation.*; *\*NTT Microsystem Integration Laboratories, NTT Corporation, Kanagawa, Japan*

3:10 p.m.

**End of Session H**

3:10 p.m. - 3:40 p.m. **Coffee Break**

**Tuesday, October 26, 2004**

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**PANEL SESSION 3:**

**III-V Foundries Pure-play vs Captive  
Joint Session with CS-MAX**

1:20 p.m. - 3:10 p.m.

**De Anza II – Portola Plaza**

**Moderators:** Walter Wohlmuth, *TriQuint Semiconductor*  
John Martinez, *BAE Systems*

The compound semiconductor industry continues to support many Foundries both captive and pure-play. How do each of these business models continue to exist as margins plummet and competition continues to become more ferocious between the III-V Foundries? Will mergers, strategic alliances, research funding and emerging markets continue to support each business model? How are new and next generation process technologies developed within each business model in regards to product optimization, device modeling and reliability qualification? What markets can each competitor compete within?

Handset  
WLAN/Wi-MAX  
mmW  
Opto/Optoelectronic

The panelists will present their current technology offerings, business models, and indications on developments for new technologies, materials and applications. Issues related to wafer and mask plate costs, cycle times, uniformity and repeatability, reliability and quality, component integration and packaging evolution will be discussed.

**Panel Members:**

Morad Chertouk *Suntek*  
Robert Donahue *WIN*  
Rob Christ *TriQuint*  
Marc Rocchi *OMMIC*  
Gopal Raghavan *InPhi*  
David Wang *GCS*

3:10 p.m. - 3:40 p.m. **Coffee Break**

**SESSION I: Advanced Silicon Transceiver ICs**

3:40 p.m. – 5:10 p.m.

**De Anza I – Portola Plaza**

**Chairpersons:** Joy Laskar, *Georgia Institute of Technology*  
Madjid Hafizi, *Nokia*

3:40 p.m.

I.1 **The Integration of High Performance Radios in Deep Sub-Micron Digital CMOS Processes (Invited)**  
Nathan Belk, *Texas Instruments R&D Center*

**Tuesday, October 26, 2004**

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4:10 p.m.

**I.2 SiGe BiCMOS 65-GHz BPSK Transmitter and 30 to 122 GHz LC-Varactor VCOs with up to 21% Tuning Range (Invited)**

C. Lee, T. Yao, M. A. Copeland\*, and S. P. Voinigescu, *ECE Department, University of Toronto, Toronto, ON, M5S 3G4, Canada*, \*Professor Emeritus, *Carleton University, Ottawa, ON, Canada*

4:40 p.m.

**I.3 Dual-Mode Direct-Conversion RF Receiver with IIP2 Calibration**

M. Hotti, J. Kaukokuuori, J. Ryyänen, J. Jussila, K. Kivekäs, K. Halonen, *Electronic Circuit Design Laboratory, Helsinki University of Technology, Helsinki, Finland*

5:00 p.m.

**End of Session I**

**SESSION J: High Power Technologies**

3:40 p.m. – 5:10 p.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Julio Costa, *RF Micro Devices*  
William Peatman, *ANADIGICS, Inc.*

3:40 p.m.

**J.1 RF-LDMOS: A Device Technology for High Power RF Infrastructure Applications (Invited),**

W. Burger, H. Brech, D. Burdeaux, C. Dragon, G. Formicone, M. Honan, B. Pryor, X. Ren, *RF Division, Networking and Computing Systems Group, Freescale Semiconductor, Tempe, AZ*

4:10 p.m.

**J.2 High Performance AlGaIn/AlN/GaN HEMTs Grown on 100-mm-diameter Epitaxial AlN/Sapphire Templates by MOVPE**

M. Miyoshi<sup>1,2</sup>, A. Imanishi<sup>1</sup>, H. Ishikawa<sup>1</sup>, T. Egawa<sup>1</sup>, K. Asai<sup>2</sup>, M. Mouri<sup>2</sup>, T. Shibata<sup>2</sup>, M. Tanaka<sup>2</sup> and O. Oda<sup>2</sup>,  
<sup>1</sup>*Research Center for Nano-Device and System, Nagoya Institute of Technology, Nagoya, Japan*, <sup>2</sup>*NGK Insulators, Ltd., Nagoya, Japan*

4:30 p.m.

**J.3 High Reliability GaN HEMT with SiN Passivation by Cat-CVD**

T. Kunii, Y. Kamo, M. Totsuka, Y. Yamamoto, H. Takeuchi, Y. Shimada, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, S. Nakatsuka, A. Inoue, T. Oku, T. Nanjo\*, T. Oishi\*, T. Ishikawa, and Y. Matsuda, *High Frequency & Optical Device Works, Mitsubishi Electric Corporation, Hyogo, Japan*, \**Advanced Technology R&D Center, Mitsubishi Electric Corporation, Hyogo, Japan*

**Tuesday, October 26, 2004**

4:50 p.m.

**J.4 Temperature-dependence of a GaN-based HEMT monolithic X-band low noise amplifier**

R.S. Schwindt<sup>1</sup>, V. Kumar<sup>1</sup>, O. Aktas<sup>2</sup>, J.-W. Lee<sup>3</sup> and I.

Adesida<sup>1</sup>, <sup>1</sup>*Micro and Nanotechnology Laboratory and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois USA,*

<sup>2</sup>*Department of Electrical and Electronics Engineering, Bilkent University, Ankara, Turkey,* <sup>3</sup>*Department of Radio Communication Engineering, Kyung Hee University, Suwon, South Korea*

5:10 p.m.

**End of Session J**

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**CS-Week 2004 Technology  
Exhibition Opening  
Reception  
Serra Ballroom  
5:00 p.m. - 7:00 p.m.**

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**Wednesday, October 27, 2004**

**REGISTRATION AND CONTINENTAL BREAKFAST**

7:00 a.m.- 12:00 noon

**Registration – Portola Lobby**

7:00 a.m. - 8:00 a.m.

**Continental Breakfast - De Anza Foyer**

**SESSION K: Beyond 100 GB/s**

**8:00 a.m.-10:00 a.m.**

**De Anza I – Portola Plaza**

**Chairpersons:** Sorin Voinigescu, *University of Toronto*  
Anu Mahajan, *TriQuint Semiconductor*

8:00 a.m.

**K.1 Transistor and circuit design for 100-200 GHz ICs (Invited),**  
M. Rodwell<sup>1</sup>, D. Scott<sup>1</sup>, M. Urteaga<sup>2</sup>, M. Dahlström<sup>1</sup>, Z. Griffith<sup>1</sup>, Y. Wei<sup>1</sup>, V. Paidi<sup>1</sup>, N. Parthasarathy<sup>1</sup>, R. Pierson<sup>2</sup>, P. Rowell<sup>2</sup>, B. Brar<sup>2</sup>, S. Lee<sup>3</sup>, N. Nguyen<sup>3</sup>, and C. Nguyen<sup>3</sup>,  
<sup>1</sup>*ECE Department, University of California, Santa Barbara,*  
<sup>2</sup>*Rockwell Scientific Company, Thousand Oaks, CA,* <sup>3</sup>*Global Communication Semiconductors, El Segundo, CA*

8:30 a.m.

**K.2 Design and InP HEMT Technology for Ultra-High Speed Digital ICs with beyond 80-Gbps Operation (Invited)**  
T. Suzuki, Y. Kawano, Y. Nakasha, T. Takahashi, K. Makiyama, T. Hirose, and M. Takikawa, *FUJITSU LABORATORIES LTD., 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan.*

9:00 a.m.

**K.3 A 132Gb/s 4:1 Multiplexer in 0.13 $\mu$ m SiGe-Bipolar Technology (Invited)**  
Mounir Meghelli, *IBM T. J. Watson Research Center, 1101 Kitchawan Road/Rte 134, Yorktown Heights, NY 10598*

9:30 a.m.

**K.4 100-Gb/s 2 7 -1 and 54-Gb/s 2 11 -1 PRBS Generators in SiGe Bipolar Technology**  
Herbert Knapp, Martin Wurzer, Werner Perndl, Klaus Aufinger, Thomas F. Meister, Josef Böck, *Infineon Technologies, CPR HF, 81730 Munich, Germany*

9:50 a.m.

**End of Session K**

10:00 a.m. - 10:20 a.m.

**Coffee Break**

**Wednesday, October 27, 2004**

**SESSION L: HBT Technology**

8:00 a.m.-10:00 a.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Chris Nordquist, *Sandia National Labs*  
Jan-Erik Mueller, *Infineon Technologies*

8:00 a.m.

L.1 **Integration of RF Front-End Modules in Cellular Handsets (Invited)**  
W-C Albert Gu, *TriQuint Semiconductor - Sawtek Division*  
*Apopka, FL*

8:30 a.m.

L.2 **Monolithic GaAs PHEMT MMICs Integrated with RF MEMS Switches (Invited)**  
J.B. Hacker, M. Kim\*, R.E. Mihailovich, and J.F. DeNatale,  
*Rockwell Scientific, Thousand Oaks, \*EE Department, Korea*  
*University, Seoul, Korea*

9:00 a.m.

L.3 **Recent Progress on Packaging of RF MEMs (Invited)**  
T. Seki, *Omron Corporation, Advanced Development*  
*Laboratory, Corporate Research and Development, Kyota,*  
*Japan*

9:30 a.m.

L.4 **Hot Via-interconnects: A Step toward Surface Mount Chip Scale Packaged MMICs up to 110 GHz,**  
Bessemoulin, A., *United Monolithic Semiconductors SAS, Orsay*  
*Cedex, France.*

9:50 a.m.

**End of Session L**

10:00 a.m. - 10:20 a.m.

**Coffee Break**

**SESSION M: CMOS, GaAs and InP for 40GB/s**

10:20 a.m. –11:30 a.m.

**De Anza I – Portola Plaza**

**Chairpersons:** Herbert Knapp, *Infineon Technologies*  
Marko Sokolich, *HRL*

10:20 a.m.

M.1 **2-to-1 Selector IC in 90-nm CMOS Technology operating up to 50 Gb/s (Invited)**  
T. Yamamoto, D. Yamazaki, M. Horinaka, and H. Onodera  
*Fujitsu Laboratories LTD1-1, Kamikodanaka 4-Chome,*  
*Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588, Japan*

## Wednesday, October 27, 2004

10:50 a.m.

M.2 **Low Supply Voltage Operation of 40-Gb/s Full-rate 4:1 Multiplexer Based on Parallel-Current-Switching Latch Circuitry**

Y. Amamiya, Y. Suzuki, Z. Yamazaki,  
M. Mamada, and H. Hida,  
*System Devices Research Laboratories, NEC Corporation*  
34 Miyukigaoka, Tsukuba, Ibaraki 305-8501, Japan

11:10 a.m.

M.3 **A 40-Gbit/s-class Universal Logic Interfacer IP Using GaAs HBT's for Heterogeneous Logic/Device Systems in Package**

T. Otsuji, S. Takahashi, N. Hamasuna, T. Takada†, Y. Matsuo†, *Kyushu Institute of Technology*, †*Anritsu Corporation*, 680-4 Kawazu, Iizuka, Fukuoka, 820-8502 Japan  
1800 Onna, Atsugi, Kanagawa, 243-8555 Japan

11:30 a.m.

**End of Session M**

### **SESSION N: MMIC Mixers and Multipliers**

10:20 a.m. – 12:00 a.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Paul Blount, *Hittite Microwave Corp.*  
Dan Scherrer, *Agilent Technologies*

10:20 a.m.

N.1 **Integrated LNA-Sub-harmonic Mixer for 77 GHz Automotive Radar Applications Using GaAs pHEMT Technology**

D. T. Bryant, R. A. Eye, D. Allen, *TriQuint Semiconductor*,  
Texas, Richardson, TX

10:40 a.m.

N.2 **A 76 GHz High Performance Subharmonic Mixer MMIC using Low 1/f Noise Diodes for Automotive Radars**

K. Kanaya, Y. Aihara, Y. Kako, H. Shutoh, T. Katoh, M. Komaru, and Y. Matsuda, *High Frequency and Optical Device Works, Mitsubishi Electric Corporation*, 4-1 Mizuhara, Itami, Hyogo 664-8641, Japan

11:00 a.m.

N.3 **Microwave Mixers based on a novel Zero Bias Diode**

M. Poppe†, D. Kleen, H. Jansson, H. Zirath\*, A. Ådahl\* *Saab Ericsson Space AB, Mölndal, Sweden*, \**Chalmers University of Technology, Göteborg, Sweden*

11:20 a.m.

N.4 **A Frequency Doubler MMIC with a Small 2-Band Elimination Filter**

Yo Yamaguchi, Tadao Nakagawa and Katsuhiko Araki  
*NTT Network Innovation Laboratories, NTT Corporation*,  
Hikarino-oka, Yokosuka-shi, Kanagawa, 239-0847, Japan

Wednesday, October 27, 2004

11:40 a.m.  
End of Session N

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**CS-Week 2004 Technology  
Exhibition Lunch  
Serra Ballroom  
11:40 a.m. – 1:00 p.m.**

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**PANEL SESSION 4:**  
**When Will The 40G Market Materialize?**

1:00 p.m. - 2:30 p.m.  
**De Anza I – Portola Plaza**

**Moderators:** Bob Cordell, *Northrup Grumman*  
Anu Mahajan

This panel will take on the question of when the market for 40 Gb/s systems, equipment, and semiconductors will become an economic reality. This is an important question for our industry, as 40 G is an important technology driver and high-speed IC consumer. This panel will focus more on market drivers and system/network issues that will influence the 40G market rather than on IC technical issues. It is anticipated that a better understanding of these higher-level issues will help IC designers prioritize their design choices.

**Panel Members:**  
YK Chen *Lucent*  
Benny Mikkelsen *Mintera*  
Kuniaki Motoshima *Mitsubishi*  
Ross Saunders *Stratlight*  
Wolfgang Templ *Alcatel*

2:30 p.m. – 3:00 p.m.  
**Coffee Break**

Wednesday, October 27, 2004

**PANEL SESSION 5 :  
mmW Technology Free For All**

1:00 p.m. - 2:30 p.m.

**De Anza II – Portola Plaza**

**Organizers/Moderators:** Paul Blount, *Hittite Microwave*  
Dan Scherrer, *Agilent Technologies*

The mmW market still seems to be waiting for the hockey stick growth curve we all expected years ago. This panel will ask, which technology will be in place when it does take off and are the two fundamentally linked. Will mmW grow when GaAs goes? What are the limiting factors for the industry? Are we in a chicken-egg situation where prices are high because demand is low and demand is low ..... What would happen if the price of a mmW chipset halved?

The panelists will present their view of the future and how their technology is likely to hit the puck...

**Panel Members:**

Jonas Bjerger *Ericsson*  
Jim Carroll *TriQuint Semiconductor*  
Chinh Doan *UC Berkeley*  
Sorin Voinigescu *University of Toronto*  
Colin Whelan *Raytheon RF Components*

2:30 p.m. – 3:00 p.m.

**Coffee Break**

**SESSION O: Modeling**

3:00 p.m. – 4:30 p.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Peter Asbeck, *University of California San Diego*  
Dave Halchin, *RF Micro Devices*

3:00 p.m.

**O.1 Device Modeling of III-V Compound Semiconductors – an Overview (Invited)**

D. E. Root, M. Iwamoto, and J. Wood, *Agilent Worldwide Process and Technology Centers, Santa Rosa, CA*

3:30 p.m.

**O.2 Physically Based Analytical Modeling of BaseCollector Charge, Capacitance and Transit time of III-V HBT's**

R. van der Toorn, J.C.J. Paasschens, R.J. Havens, *Philips Research Laboratories, Eindhoven, The Netherlands*

## Wednesday, October 27, 2004

3:50 p.m.

O.3 **Simulation of Gate Lag and Current Collapse in GaN HFET**

N. Braga<sup>1</sup>, R. Mickevicius<sup>1</sup>, R. Gaska<sup>2</sup>, M. S. Shur<sup>3</sup>, M. Asif Khan<sup>4</sup>, and G. Simin<sup>4</sup>.

<sup>1</sup>*Integrated Systems Engineering Inc., San Jose, CA*, <sup>2</sup>*Sensor Electronic Technology Inc., Columbia, SC*

<sup>3</sup>*Electrical, Computer, and Systems Engineering Dept, Rensselaer Polytechnic Institute, Troy, NY*

<sup>4</sup>*Department of Electrical Engineering, University of South Carolina, Columbia, SC*

4:10 p.m.

O.4 **Low Phase Noise 2 Ghz Hbt Push-Push Vco Based On An Advanced Low Frequency Noise Model**

<sup>1</sup>P. Cortese, A. Sion, <sup>2</sup>M. Prigent, <sup>1</sup>*UMS S.A.S., Orsay Cedex, France*, <sup>2</sup>*IRCOM – CNRS, Brive, France*

4:30 p.m.

**End of Session O**

### **SESSION P: Millimeter Wave MMICs**

3:00 p.m. – 4:30 p.m.

**De Anza II – Portola Plaza**

**Chairpersons:** Yves Bayens, *Lucent Bell Labs*  
Dan Scherrer, *Agilent Technologies*

3:00 p.m.

P.1 **A 220 GHz Metamorphic HEMT Amplifier MMIC**

A. Tessmann, A. Leuther, H. Massler, M. Kuri, C. Schwoerer, M. Schlechtweg, and G. Weimann, *Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany*

3:20 p.m.

P.2 **A 110-GHz AISb/InAs MMIC Amplifier**

W.R. Deal, R. Tsai, M. Lange, J.B. Boos\*, B. Bennet\*, R. Grundbacker, L.J. Lee, K. Padmanabhan, P.H. Liu, C. Namba, P. Nam and A. Gutierrez, *Northrop Grumman Space Technology, Inc., Redondo Beach, CA*; \**Naval Research Laboratory, Washington, DC*

3:40 p.m.

P.3 **Broadband Low-Noise Amplifiers for K- and Q-Bands Using 0.2  $\mu$ m InP HEMT MMIC Technology**

R. Limacher, L. Scoca, T. Zaugg, H. Meier, A. Megej, A. Orzati, and W. Bächtold, *Laboratory for Electromagnetic Fields and Microwave Electronics, Swiss Federal Institute of Technology (ETH), CH-8092 Zurich, Switzerland.*

4:00 p.m.

P.4 **High-Gain Direct-Coupled Matrix Distributed Amplifier Using Active Feedback Topology**

W. Ko and Y. Kwon, *School of Electrical Engineering, Seoul National Univ, Seoul, S. Korea*

**Wednesday, October 27, 2004**

4:20 p.m.

P.5 **A Very Compact 60GHz Transmitter Integrating GaAs  
MMICs on LTCC Passive circuits for Wireless  
Communications Applications**  
Y. C. Lee, W. Chang, Y. C. Chul, S. Park, *School of  
Engineering, Information and Communications University  
(ICU), Daejeon, Korea*

4:40 p.m.

**End of Session P**

5:00 p.m.

**Close of Symposium**

# 2004 IEEE CSIC Symposium Organizers

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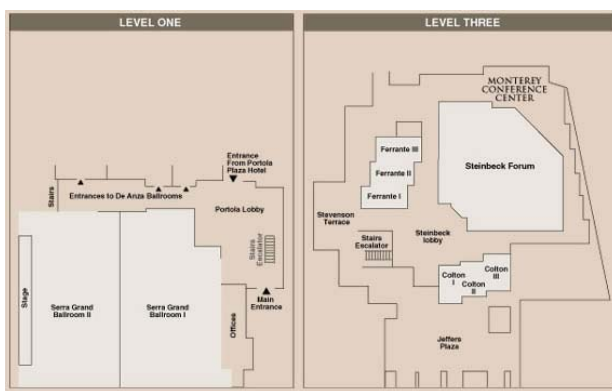
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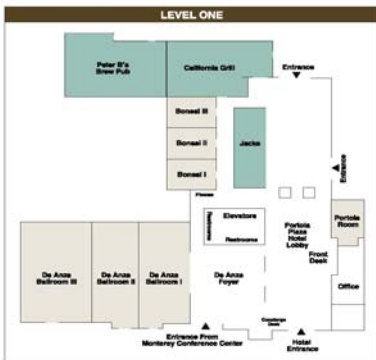
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