InP HBT Integrated Circuit Technology with Selectively Implanted Subcollector and Regrown Device Layers[1]

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Abstract – We describe a quasi-planar HBT process using a patterned implanted subcollector with a regrown MBE device layer. Using this process we have demonstrated discrete SHBT with f_t > 250 GHz and DHBT with f_t > 230 GHz. The process eliminates the need to trade base resistance for extrinsic base/collector capacitance. The low proportion of extrinsic base/collector capacitance enables further vertical scaling of the collector even in deep submicron emitters thus allowing for higher current density operation. Demonstration ring oscillators fabricated with this process had excellent uniformity and yield with gate delay as low as 7 ps and power dissipation of 6 mW/CML gate. At lower bias current the power delay product was as low as 20 fJ. To our knowledge, this is the first demonstration of high performance HBTs and integrated circuits using a patterned implant on InP.

I. INTRODUCTION

InP-based HBT have gained wide acceptance for relatively high transistor count (>1000 HBT) circuits for a number of applications[1,2,3,4]. Power dissipation of logic gates at multi-GHz clock rates continues to be an issue of concern with all III-V HBT because of their relatively large feature size (~10µm^2 emitter area). High power dissipation is the main limitation to realizing significantly larger circuits at 50+ GHz clock rates. Traditional InP HBT mesa structure devices have epitaxial layers more than 1µm thick and therefore have lateral dimensions that are of the same order. Further scaling below about 2µm^2 using the mesa structure does not seem to yield improved power-delay product. In the mesa structure the lack of flexibility to independently scale the *lateral* base contact and the *vertical* collector contact results in compromises in device fabrication. Inability to scale to deep submicron dimensions has made it difficult to fully exploit the material properties of InP to obtain high speed, high density integrated circuits with reasonable power dissipation.

In this paper we describe an IC process with selectively implanted subcollector and MBE regrown InP HBT device layers that circumvents the scaling issues common to mesa isolated transistors. Subcollector patterning allows for device isolation without the need for a deep mesa etch. As a result, the HBTs described in this paper are more nearly planar and more compatible with high density interconnect. Heat spreading is also more efficient because of both the material[5] (InP instead of InGaAs) and the geometry of the subcollector. Patterning of the subcollector implant reduces the need to make the base mesa small to reduce junction capacitance. Furthermore, the smallest lateral dimensions of the HBT can now be reduced without significantly affecting circuit yield. Submicron (0.5x4 µm^2) transistors built using such a process had current gain cutoff frequency in excess of 250 GHz and maximum frequency of oscillation in excess of 120 GHz.

Because little or no performance penalty occurs in scaling the emitter width from micron to submicron dimensions, smaller devices perform nearly as well as larger devices. The device structure is fully compatible with a standard IC process. We demonstrate IC compatibility with 31 stage CML ring oscillators containing about 100 transistors. The measured gate delay was as low as 7 psec with a power dissipation of < 6mW. Yield and uniformity of the oscillation frequency were as good or better than results obtained on similarly prepared mesa etch wafers. To our knowledge, this is the first demonstration of cutoff frequency in excess of 200 GHz on scalable ion implanted InP HBTs and the first demonstration of integrated circuits using such a process.

II. EPITAXIAL STRUCTURE AND FABRICATION

The three mesa process for III-V HBTs requires that MBE layers in the upper mesas overlap all MBE layers below. In particular the heavily p-doped base and the heavily n-doped subcollector overlap over the entire extent of the base/collector mesa. This overlap (plus fringing effects) determines the total base/collector capacitance. In deep submicron devices only a small portion of this mesa represents the intrinsic transistor and only this portion *requires* a subcollector contact. An implant allows the placement of the

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subcollector only where it is required as shown in Fig. 1. The planar process results in 2 distinct reductions of the overall device vertical dimension resulting in a quasi-planar transistor. The first reduction comes from the direct omission of the isolation mesa etch to remove the heavily doped subcollector between transistors. The second reduction comes from the scaling of the collector made possible by the reduction in extrinsic overlap area of the base and subcollector. In our device the mesa height was reduced from 1.1 µm to < 0.6 µm.

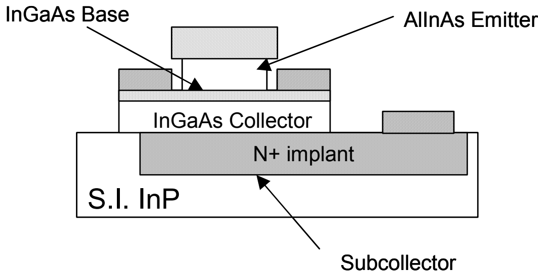

Figure 1-Schematic cross section of device structure.

To realize the patterned subcollector, Si was implanted at 80 keV ($2.5x10^{14}$ /cm^2) and 240 keV ($5x10^{14}$ /cm^2) into masked S.I. InP substrates. Mask openings as small as 0.25µm were used. The mask was then removed and the wafers annealed with a phosphine overpressure at 700C. A SIMS profile from a companion wafer is shown in Fig. 2. The AlInAs/InGaAs/(InGaAs or InP) epitaxial structures for this work were grown by gas source molecular beam epitaxy (GSMBE). All layers were grown lattice matched on semi-insulating InP substrates and the p-type and n-type dopants were beryllium and silicon, respectively. The basic SHBT structure has been reported previously[8]. The MBE growth omitted the subcollector (now realized by implantation) and reduced the collector thickness to 100 nm. The MBE profile of the DHBT device is shown in Fig. 3.

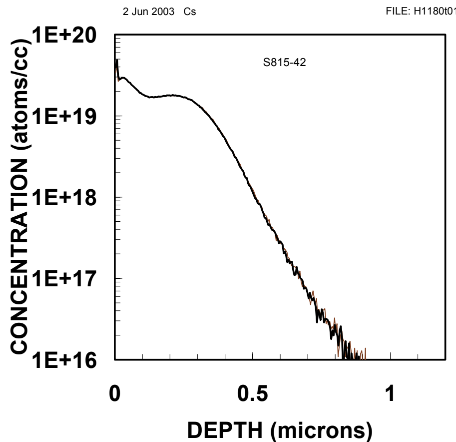

Figure 2- SIMS depth profile of Si implanted subcollector.

Layer description		Thickness (Å)	Doping Level (cm^{-3})
MBE	InGaAs contact	1100	n:2.1E19
MBE	InAlAs emitter contact	400	n:1.0E19
MBE	InAlAs emitter	1050	n:1.3E18
MBE	Chirped SLs	231	n:1.3E18
MBE	InGaAs base layer	325	p:2.9E19
MBE	Quaternary grade InP Collector	980	n:1.0E17

Figure 3-Schematic DHBT MBE layer structure (Implanted subcollector not shown).

Emitters with measured dimensions as small as 0.35 µm were patterned on the wafer. The base dimensions could be made arbitrarily large without much impact to the base/collector capacitance but 0.5 µm was considered sufficient to minimize base contact resistance. Measured base contact resistivity (from TLM patterns) was $2x10^{-7}$ Ωcm^2. The base sheet resistance was 650 Ω/□. Emitter access resistance was 20 Ω µm^2 including both contact and bulk semiconductor resistance of the emitter cap. The subcollector sheet resistance was about 22 Ω/□. Other details of the process have been reported previously[6]. The interlayer dielectric was planarized in an Inductively Coupled Plasma (ICP) etcher which is also used to define the via contacts[7].

The mask used to pattern devices on this lot was not fully optimized for the implantation and so did not contain the minimum base/collector overlap possible. However, the results in the next section indicate that the process is IC compatible and preserves yield and uniformity of HBTs.

III. DEVICE PERFORMANCE

A forward Early characteristic of a 0.5x4 µm^2 SHBT transistor is shown in figure 4. Current gain for this device was well over 150 indicating a very high quality base-layer growth on the implanted substrate. Maximum current density in the devices was about 700 kA/cm^2. Breakdown (BVceo) on the SHBT transistors with 100nm collector was 3.1V. A similar characteristic is shown in figure 5 for a DHBT grown on a wafer from the same implant lot. The current gain is somewhat lower but the breakdown is much higher at about 4.5V. The maximum current gain for the DHBT was greater than 70. These high values of current gain indicate that the base layer was of extremely high quality even though significant wafer processing occurred before the MBE growth.

We obtained 250 GHz f_t on SHBTs and 230 GHz f_t on DHBTs (V_{ce} = 1V, I_c = 10 mA). Fig. 6 shows the extrapolated f_t from de-embedded s-parameter measurements to 110 GHz. Fig. 7 shows the f_t dependence on device current (approximate emitter area = 2 µm^2). The f_t extrapolations in Figure 7 are from single frequency measurement at 40 GHz at each current bias. The collector emitter potential (Vce) for the measurements in Fig. 7 was 1.5V.

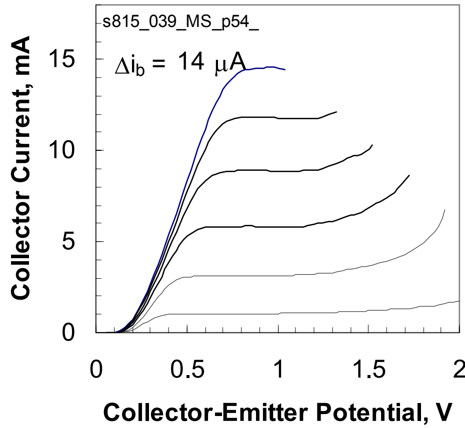

Figure 4-Forward Early characteristic of 0.5x4µm^2 InP SHBT with implanted subcollector.

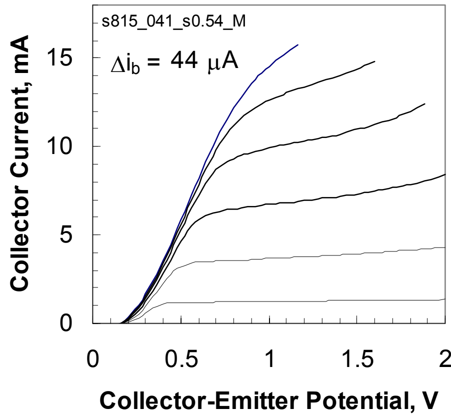

Figure 5-Forward Early characteristic of 0.5x4µm^2 InP DHBT with implanted subcollector.

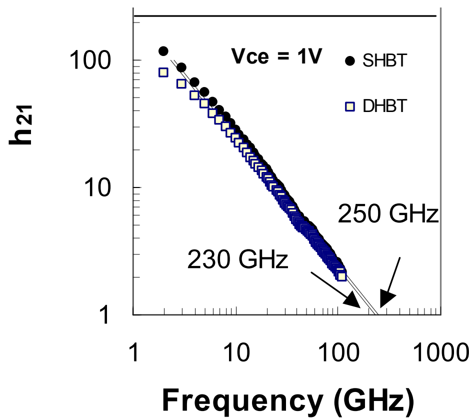

Figure 6-De-embedded h_{21} as a function of frequency for both SHBT and DHBT devices with implanted subcollector.

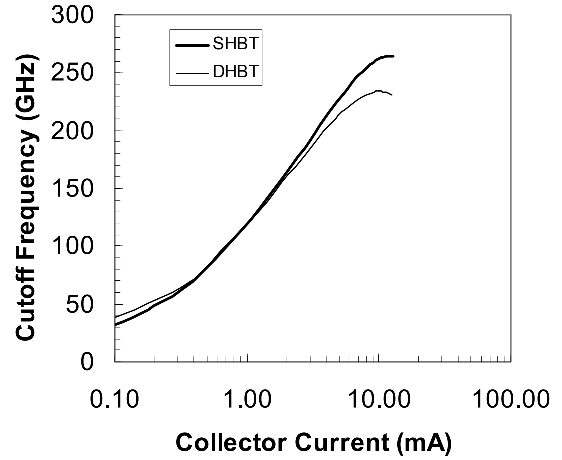

Figure 7-Unity current gain cutoff frequency (*f_t*) of 0.5x4 µm^2 InP SHBT and DHBT with implanted subcollector.

IV. Circuit Performance

A key motivation to use implanted subcollector HBTs instead of further scaled mesa HBTs is to achieve performance gains without sacrificing IC producibility or yield. In this section we review early circuit results from demonstration vehicles using a 2-level metal process.

A number of 15 and 31-stage ring oscillators were tested with device sizes ranging from 0.35x1 µm^2 to 1x3 µm^2. Load resistors in the CML gates were realized by ion implantation. Figure 8 is a photomicrograph of one of the 31-stage ring oscillator circuits (utilizing 0.5x4 µm^2 HBT described previously). Gate delay and power dissipation for a range of bias currents (externally applied) is shown in figure 9. Note that the logic swing changes but is > 250 mV for bias current above 2.5 mA/stage.

Because our new process requires substantial modification to the growth of the device epitaxial material, one of our priorities was to investigate the uniformity and yield of transistors. The ring oscillators provide a simple method to evaluate both. Figure 10 shows the distribution of calculated CML gate delay of 31-stage ring oscillators on the SHBT wafer. The yield of these 100 transistor circuits was excellent with significant clustering so that there was no yield loss attributable to HBTs in the center 80% of the wafer. The yield results give further indication that the MBE epitaxial layers were of very high quality. Given these yield and uniformity results we would expect demonstration circuits with 1000 transistors to be possible.

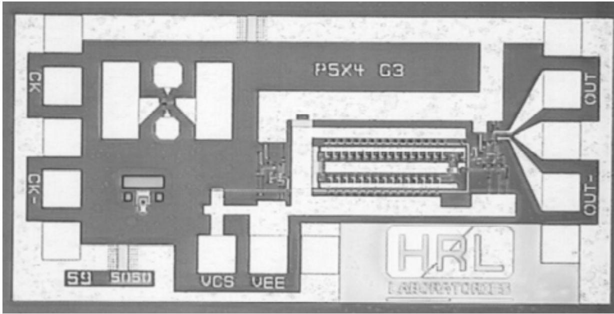

Figure 8-31-stage ring oscillator circuit employing the 0.5x4µm SHBT and CML inverters. The circuit contains about 100 SHBTs.

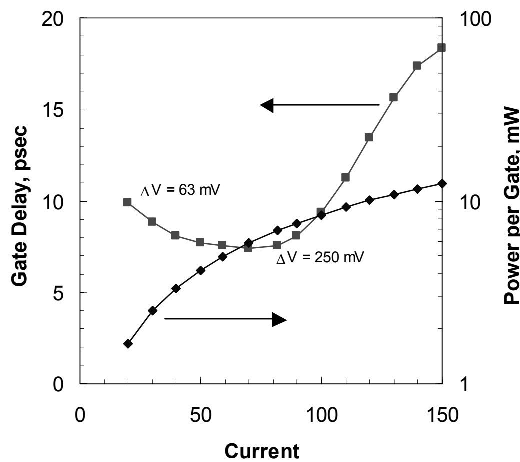

Figure 9-Gate delay and power dissipation per gate extracted from 31-stage ring oscillator as a function of total circuit current. Vee = -3.0 V.

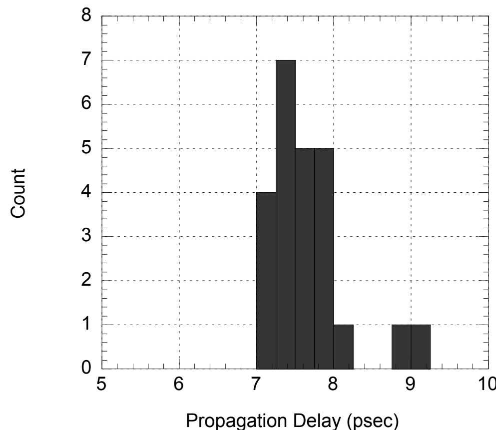

Figure 10-Distribution of CML gate delay on one wafer.

The yield and uniformity results are comparable to our mesa HBT processes. The gate delay is greater than we had previously reported[8] on mesa HBT with similar structures mainly due to non-optimum load resistances defined by the subcollector implant. In this case power delay product is a better comparison of the circuit performance. Power delay product was as low as 20 fJ which is comparable to the mesa HBT process with the same device geometry.

V. SUMMARY

We have demonstrated an integrated circuit process utilizing a patterned ion implantation step to define the HBT subcollector. High quality MBE material comparable to that grown on virgin InP substrates has been grown on the annealed surface. Using this process we have demonstrated devices with unity current gain cutoff frequency (f_t) as high as 250 GHz. We have also demonstrated highly uniform device characteristics and yield at the 100 HBT level with ring oscillators. The ring oscillators had gate delay as low as 7 psec and power delay product as low as 20 fJ. Through further optimization of the base/subcollector overlap, this technology has the potential of producing high yield, high performance HBTs with deep submicron dimensions.

VI. ACKNOWLEDGEMENT

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