

# A LOW POWER 72.8 GHz STATIC FREQUENCY DIVIDER IMPLEMENTED IN AllnAs/InGaAs HBT IC TECHNOLOGY

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**Abstract** – We report a 72.8 GHz fully static frequency divider in AllnAs/InGaAs HBT IC technology. The CML divider operates with a 350 mV logic swing at less than 0dBm input power up to a maximum clock rate of 63 GHz and requires 8.6 dBm of input power at the maximum clock rate of 72.8GHz. Power dissipation per flip-flop is 55mW with a 3.1V power supply. To our knowledge this is the highest frequency of operation for a static divider in any technology. The power-delay product of 94 fJ/gate is also the lowest power-delay product for a circuit operating above 50GHz in any technology. A low power divider on the same substrate operates at 36 GHz with 6.9mW of dissipated power per flip-flop with a 3.1V supply. The power delay of 24 fJ/gate is, to our knowledge, the lowest power delay product for a static divider operating above 30GHz in any technology.

## I. INTRODUCTION

InP based HBT technology is gaining momentum for a wide variety of very high speed digital and mm-wave applications. AllnAs/InGaAs lattice matched to InP SHBT have been successfully demonstrated in many circuit applications including 50 Gb/s 4:1 MUX<sup>1</sup>, 50 Gb/s 1:4 DMUX<sup>2</sup>, 38 GHz VCO<sup>3</sup> and 74GHz distributed amplifier<sup>4</sup>. Many of these are critical components for the next generation of 40 Gb/s communication networks.

Recently static dividers have been reported with toggle rates exceeding 60 GHz<sup>5,6</sup>. In this paper we report on the demonstration of a static divider operating at 72.8 GHz maximum toggle rate with a power dissipation of 55 mW/flip-flop. We have opted for a highly robust process that uses conventional lithography to demonstrate the type of performance that should be achievable in larger circuits. By using a modern I-line stepper we have realized excellent device and circuit performance. The improvement is due to substantial size reduction of the extrinsic elements of the transistor in comparison to our previously reported results<sup>7</sup>. Robustness of the technology is further demonstrated by the small spread in divider performance over a wafer. This work demonstrates that InP based HBTs can be produced to operate at 60GHz clock rates with substantial design margin.

## II. STATIC DIVIDER AS TECHNOLOGY BENCHMARK

Digital circuits in any high speed technology are typically benchmarked by the performance of *static* frequency dividers. Performance of a static divider is a recognized figure of merit for digital integrated circuit processes because a static frequency divider uses the same basic flip-flop elements found in more complex sequential circuits<sup>8</sup>.

A cascade of basic divider cells in a divide by four or divide by eight circuit (made of identical stages) gives a good representation of the gate delay of any flip-flop because the loading (fan out) and feedback paths are similar to more complex circuits. Ring-oscillator gate delay, on the other hand, should only be interpreted as a best-case of the *transistors* alone and not the full circuit process. Likewise quasi-static or dynamic dividers can be useful components in high frequency systems but their usefulness as technology benchmarks is limited.

Additional components in a full stand-alone divider circuit further improve the significance and applicability of the result. A broadband input buffer removes any uncertainty about the introduction of an adequate signal to the flip-flop. Likewise an appropriate output buffer assures that the last stage in the divider is under a realistic load and that the technology is reasonably capable of driving a standard output. Finally, on-board generation of the bias condition produces a realistic performance spread based on process variation. These elements together result in a circuit that is a miniature test bed that can be used to predict the performance, yield and reliability of much larger logic circuits.

Although power dissipation of a frequency divider alone is rarely a limiting factor in system designs in which dividers are used, power is an important *benchmark* of the technology because it can limit the integration level and therefore the available functionality of more complex circuits. This is especially true at the highest operating rates where power dissipation per gate is on the order of hundreds of mW.

## III. EPITAXIAL STRUCTURE AND FABRICATION

The AllnAs/InGaAs epitaxial structures for this work were grown by gas source molecular beam epitaxy (GSMBE). All

The only modification to the circuit was minor optimization of the load resistance and the insertion of the G2+ HBT in place of the G2 HBT<sup>7</sup>. The interconnect wiring was not changed.

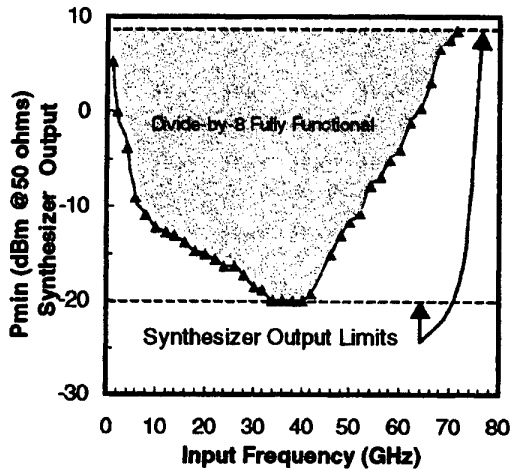


Fig. 3 – Sensitivity to input power level of 72.8GHz divider. Maximum available output power of synthesizer is 9dBm

A plot of divider sensitivity to input signal is shown in figure 3. The input power in the plot is the power provided by the signal generator and does not include cable losses to the circuit. A 50Ω through line with the same I/O configuration as the divider was used to calibrate the cable and probe card loss which was about 4dB over a wide range of frequency from 40 to 70 GHz. The divider operated with 0dBm up to 63GHz without taking account of cable losses. Taking losses into account the divider operated up to approximately 67GHz at 0dBm. Maximum toggle rate of 72.8GHz (fig. 5) was achieved with input power of less than 5dBm at the input buffer (8.6dBm from the signal generator). The differential input is terminated with 50Ω resistors to ground so that there is an additional 6dB loss of the input signal on-chip.

Figure 3 is important from a benchmarking perspective because it establishes that the circuit operates over the entire frequency range from dc to the maximum toggle rate (it was tested at 100MHz minimum). A straightforward dynamic divider using a single differential amplifier fed back to a mixer should result in frequency division from about  $f_i/3$  to  $f_i^{14}$  so showing frequency division over a limited frequency range does not establish performance of a flip-flop that is widely applicable in sequential circuits. In a static divider we would expect a maximum toggle rate of  $f_i/2$ , in this case we obtained a toggle rate of 37% of  $f_i$  which is similar to our previous result and indicates that, in the presence of device and interconnect parasitics, the delay elements have complex relationships<sup>15</sup>.

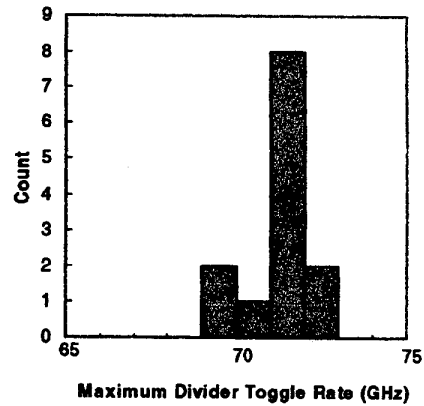


Fig. 4 – Distribution of maximum toggle rates on-wafer at a constant power supply voltage of 3.1V.

In automated probing of dividers at a fixed power supply voltage of 3.1V we obtained excellent uniformity of the toggle rate as shown in Fig. 4. This is a hallmark of HBT CML circuits.

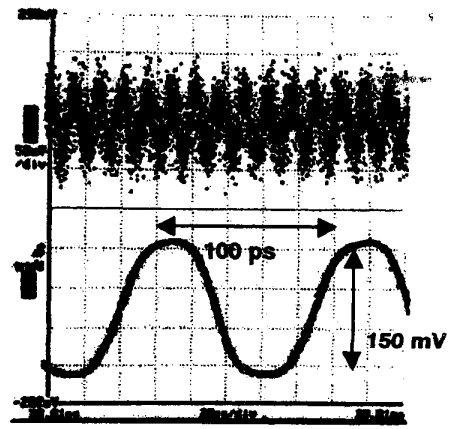


Fig. 5 – Oscilloscope display showing the divided output signal at 9.1GHz and the 72.8GHz input.

Because there is wide interest in 40 Gb/s logic circuits for communications, there is interest in a high speed digital technology with adequate process and design margin at 40GHz or 20 GHz clock rates. To address circuit applications at 20 GHz we designed a low power version of the divider with 0.5x4μm transistors in the flip flop and 0.5x2μm HBT in the input buffer. Changes to the circuit design were minimal although we did take advantage of the compactness of the smaller HBT to reduce the interconnect length. Load resistors were chosen for good speed/power tradeoff and the resulting bias current in the HBT was reduced to  $5 \times 10^4$  A/cm<sup>2</sup>.

layers were grown lattice matched on semi-insulating InP substrates and the p-type and n-type dopants were beryllium and silicon, respectively. The basic structure has been reported previously<sup>8</sup>. The only change to the basic structure was an adjustment of the collector thickness to 200nm.

The frequency dividers were fabricated in a 4  $\mu\text{m}$  wire-pitch AlInAs/InGaAs HBT IC process with dry/wet etched emitter and wet etched base and collector mesas<sup>9</sup>. The process includes a self-aligned base metal to the emitter but optically aligned collector and base contacts. Contact to the device is made with second level metal. The interlayer dielectric is polyimide, planarized in an Inductively Coupled Plasma (ICP) etcher which is also used to define the via contacts<sup>10</sup>. A scanning electron micrograph of a completed transistor structure without the device contact layer is shown in Fig. 1. The layer to layer registration required to realize the transistor in the figure is 0.1 $\mu\text{m}$  between base and emitter and between base and collector contact.

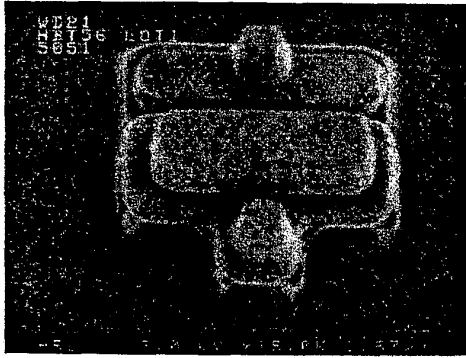


Fig. 1 – Scanning electron micrograph of 1x3mm<sup>2</sup> InP SHBT prior to device contact.

#### IV. DEVICE AND CIRCUIT PERFORMANCE

To demonstrate the effect of straightforward lithographic scaling on device performance we fabricated both standard layout (G2) HBT, which require 0.25 $\mu\text{m}$  registration accuracy, as well as reduced parasitic (G2+) devices with 0.1 $\mu\text{m}$  registration. Unity current gain cutoff frequency,  $f_t$ , of 152 GHz was measured for a standard device and 198 GHz for a reduced parasitic device (both with 1x3 $\mu\text{m}$  emitter). An  $f_{\text{max}}$  of 272 GHz was measured for the reduced parasitic device. A comparison of the performance of the two styles of HBT, adjacent on the wafer, is shown in Fig. 2.

As can be seen from the SEM, the need to make effective base contact results in a parasitic base tab structure that does not scale with emitter length. The capacitance associated with this feature is just the base collector depletion capacitance,  $C_{bc}$ , below the base tab. With a 2000A collector, the entire

collector region is depleted of charge and the capacitance is reduced to a constant parallel plate capacitance over the entire range of transistor bias. A second parallel plate parasitic capacitance that scales with emitter length is also present. This capacitance is associated with the non-zero width of the base contact around the periphery of the emitter and includes fringing capacitance. The width of the base metal is chosen to optimize the tradeoff between base resistance and base/collector capacitance and essentially results in a tradeoff between  $f_t$  and  $f_{\text{max}}$ . The only real difference between the G2 and G2+ transistors were the values of  $C_{bc}$ : 16fF for the former and 7fF for the latter.

Clearly the non-scaling  $C_{bc}$  affects small transistors much more than large transistors. Its effect becomes essentially negligible for emitter length greater than 5 $\mu\text{m}$  for the structure shown in the figure. Although there have been numerous reports of techniques to minimize parasitic capacitance using undercut<sup>11</sup>, dielectric fill<sup>12</sup> or transferred substrate<sup>13</sup>, none of the reports present results on particularly small, low current devices. Because of various process tradeoffs, these other structures are only marginal improvements over the straightforward structure and they complicate processing considerably.

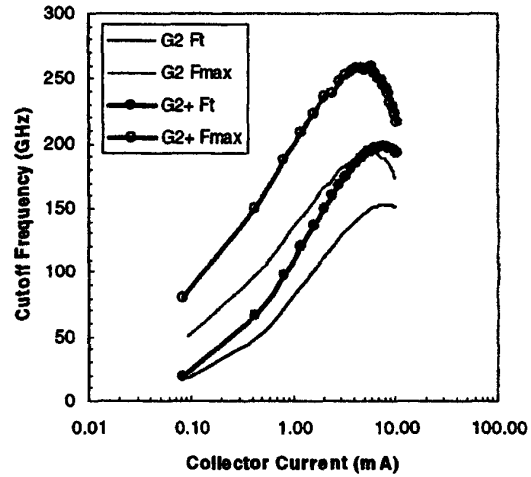


Fig. 2 – Comparison of current and power gain cutoff frequency ( $f_t$ ,  $f_{\text{max}}$ ) for 1x3  $\mu\text{m}$  emitter HBT with parasitic reduction (G2+) and standard layout.

The divider is designed around a conventional CML D flip-flop. A circuit diagram of the basic master slave flip-flop has been reported previously<sup>8</sup>. The high speed divider was designed with load and current source resistances of 35 ohms. The bias current for the divider was 9 mA or  $3 \times 10^5$  mA/ $\mu\text{m}^2$ . A micrograph of the circuit has been published previously.

Maximum toggle rate in the low power circuit was 36GHz with a 3.1V supply. The low power divider stage dissipated 6.9mW per flip-flop. This is an effective power delay product of 24 fJ if we assume 2 gate delays per flip flop and an equivalent complexity of 4 logic gates (the effective number of logic gates is only important in comparing to ring oscillators...divider comparisons are unambiguous). This power-delay product is less than one-tenth of that available in competing materials systems<sup>16,17,18</sup> for circuits operating above 20 GHz (Fig. 6).

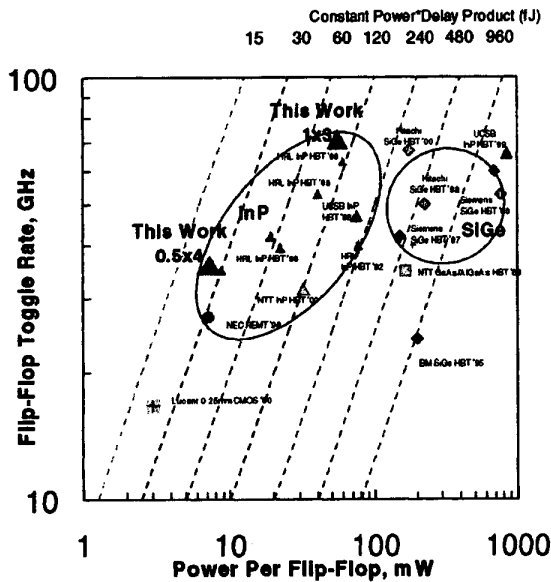


Fig. 6 – Flip-flop toggle rate vs. power dissipation for a number of dividers reported in the literature.

## V. SUMMARY

We have demonstrated a 72.8 GHz static 1/8 divider in AlInAs/GaAs technology. We believe this is the fastest static divider reported in any semiconductor technology to date. Power dissipation was 55 mW per flip-flop. The results were achieved by straightforward scaling of a face-up SHBT process. Most important to this scaling was critical layer to layer registration. Improvement over previous static divider results was primarily due to minimization of HBT extrinsic parasitic elements. No special circuit techniques were employed, instead, a known architecture and layout were used to highlight the device improvement. Evolutionary changes to InP based technology have now reached a level where 60 GHz clock rate sequential circuits with adequate design margin should be achievable. More importantly, circuits with wide design margin at 20 GHz and 40 GHz clock rates and very low power are within easy reach and should pave the way to 40 Gb/s communication chip sets.

## VI. ACKNOWLEDGEMENT

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