

An 80-Gbit/s Multiplexer IC Using InAlAs/InGaAs/InP HEMTs

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Abstract—We report on an 80-Gbit/s 2:1 selector-type multiplexer IC using InAlAs/InGaAs/InP HEMTs incorporating a high-speed double-layer interconnection process with a low-permittivity insulator. The record operating data rate was measured on a 3-inch wafer. In spite of the bandwidth limitation on the measurement setup, clear eye patterns were successfully observed for the first time.

I. INTRODUCTION

The rapid movement toward broadband ISDN and multi-media services urgently requires the expansion of transmission capacity to beyond terabit per second. In terms of system practicality, reliability and cost, we still have to improve the speed of electronic ICs to around 40 Gbit/s and more even though WDM and OTDM technologies relax the demands on the single-channel bit rate. Recently, several 40-Gbit/s class ICs have been developed [1-4] and a fully-electrical TDM (ETDM) optical fiber transmission experiment has been demonstrated at this bit rate [3, 5].

High-speed time-division multiplexers (MUXs) are key components in broadband optical fiber communication systems. To date, the highest data rate of the MUX reported so far is 64 Gbit/s on a wafer and 52 Gbit/s on a packaged module [6]. We report on the record speed performance of a 2:1 MUX IC using InAlAs/InGaAs/InP HEMTs.

II. PROCESS TECHNOLOGY

The IC process we used is a 0.1- μm gate length InAlAs/InGaAs/InP HEMT process [7, 8]. A novel InP gate-recess-etch stopper inserted into the InAlAs barrier layer dramatically improves the uniformity of the transistor performance (the average threshold voltage (V_{th}): -0.65 V with a standard deviation of less than 40 mV in a 3-inch wafer). The average transconductance, f_T , and f_{max} are 1050 mS/mm, 195 GHz, and 230 GHz, respectively.

As the device speed increases, the interconnection parasitics (propagation delay and waveform distortions due to multiple reflection) come to dominate the circuit speed performance [9]. Thus a high-speed interconnection technology together with impedance matching design is crucial. To reduce the interconnection propagation delay by making the layout

denser, small low-loss Schottky diodes using additional InAlAs/n-InAlAs layers were introduced.

In addition, we newly adopted a high-speed interconnection process using two metal layers consisting of gold and a 2- μm -thick BCB film as an inter-level dielectric with a low permittivity ($\epsilon_r = 2.8$). For example, when a microstrip line is configured with a 2- μm -wide 2nd-layer conductor on top of the 1st-layer ground, the propagation velocity along the line is 1.5 times faster than that for a line without the 1st-layer ground because the effective dielectric constant is reduced from 6.7 to 2.6 by shielding the substrate using the 1-st layer ground.

III. CIRCUIT DESIGN

Figure 1 shows the circuit block diagram of the MUX. Each block is based on the SCFL (Source-Coupled FET Logic) series-gated circuitry. Internal differential circuitry consists of 20- μm FETs and 130-ohm load resistors. All the data and clock inputs are single-ended. The input-stage source follower includes an internal 50-ohm termination resistor.

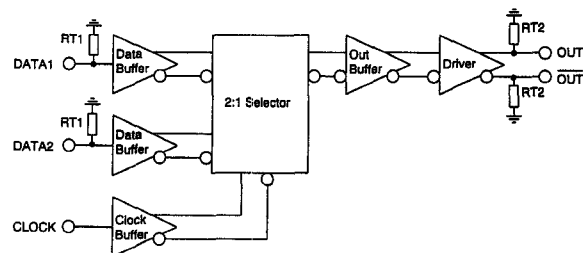


Fig. 1. Circuit block diagram of the MUX IC.

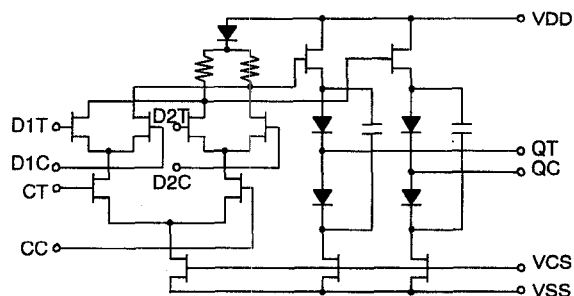


Fig. 2. Circuit diagram of the selector core.

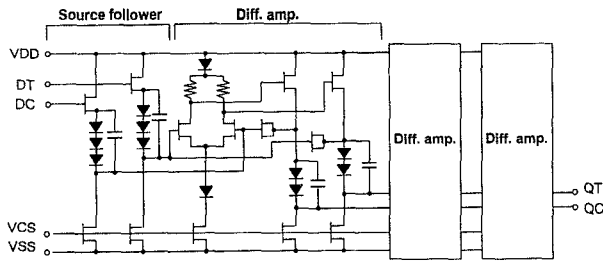


Fig. 3. Circuit diagram of the data buffer.

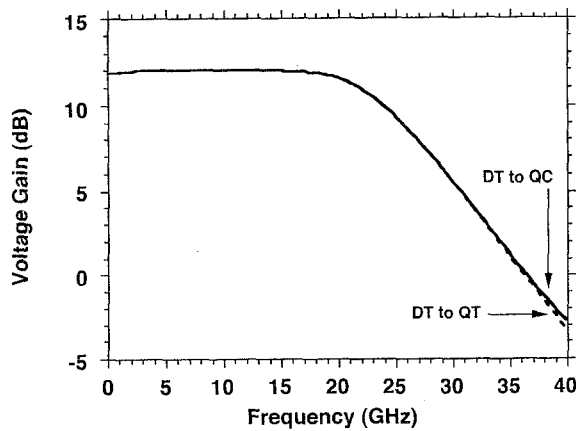


Fig. 4. Simulated gain-bandwidth characteristics of the data buffer.

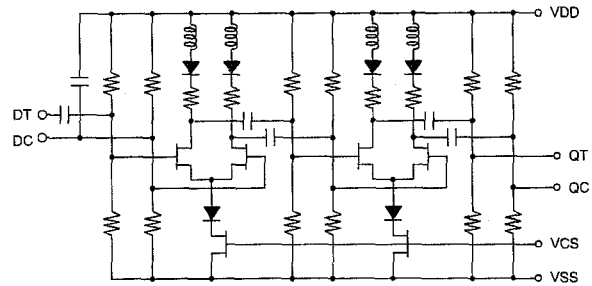


Fig. 5. Circuit diagram of the clock buffer.

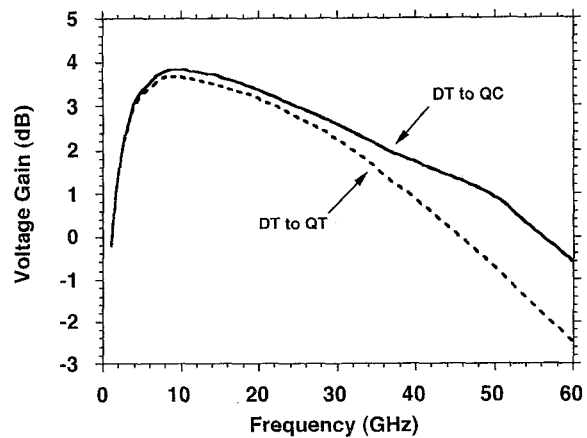


Fig. 6. Simulated gain-bandwidth characteristics of the clock buffer.

The core of the MUX is based on a simple selector circuitry (shown in Fig. 2.). Capacitive peaking was incorporated into the source followers, which compensates for the loss at high frequencies, resulting in higher speed operation.

As the core circuit operates faster, data and clock buffers should expand their bandwidth to maximize the speed performance of whole the circuit. The data input stage of the MUX was designed as a data buffer with 3 stages as shown in Fig. 3. Each of the stages consists of a capacitive-feedback differential amplifier [10] and a couple of source followers with capacitive peaking. The capacitive feedback cancels the influence of the parasitic gate capacitance. A simulated gain-bandwidth of the data buffer is shown in Fig. 4. This input stage has a -3-dB bandwidth of 25 GHz with a DC voltage gain of 12 dB, which assures >35-Gbit/s NRZ data equalization.

The circuit diagram of the clock buffer, which consists of a two-stage inductor peaking differential buffer, is shown in Fig. 5. A capacitively-coupled

resistive divider was introduced as a low-loss passive RF level shifter instead of source followers. The lower cut-off frequency of the divider was designed at less than 2 GHz so that a wide operating range from <2 to >40 GHz was obtained. A simulated gain-bandwidth of the clock buffer is shown in Fig. 6.

The high-speed interconnection using a microstrip line with a 2- μm -wide 2nd-layer conductor on top of the 1st-layer ground was introduced to the inter-block connection from the data buffer to the selector core and from the clock buffer to the selector core. The physical lengths of these connections are 400 μm and 330 μm , respectively. The high-speed interconnection helped reduce their electrical lengths below one tenth of the wavelength at frequencies of up to 50 GHz. In addition, the characteristic impedance of the microstrip line is very low (42 Ω) compared to the conventional line without 1st-layer ground (~180 Ω), which results in a better matching with the low output impedances (~25 Ω and ~60 Ω) of the data and clock buffers. These are keys to achieving high-speed circuit operation near 100

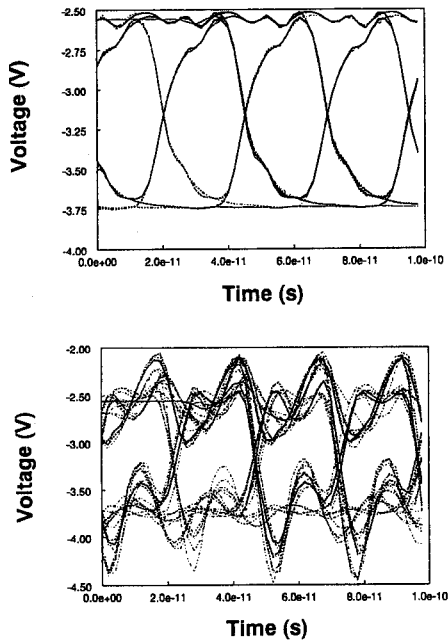


Fig. 7. Simulated eye diagrams at the data input node of the selector core circuit for 40-Gbit/s PRBS data.

Upper: high-speed interconnection; lower: conventional.

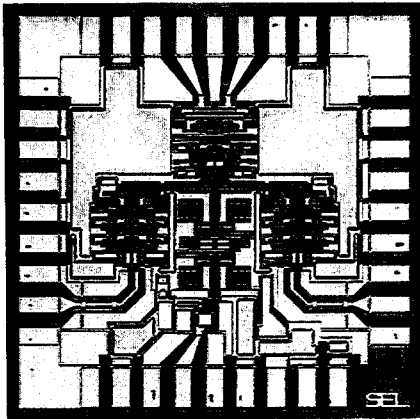


Fig. 8. Microphoto of the MUX IC (2 mm x 2 mm.).

Gbit/s. Figure 7 shows simulated 40-Gbit/s waveforms at the data input node of the selector core circuit. The signal distortions due to multiple-reflection along the interconnection lines are well suppressed for the high-speed interconnection, whereas in a conventional case, the distortions are severe.

The output stage consists of a series of a 2-stage buffers (20- μm FETs for the first stage and 40- μm FETs for the second one) and a driver (70- μm FETs) with impedance-matched termination resistors at the differential output drain nodes. The power supply voltage is -5.2 V. The chip consumes 2.7 W. The chip size is 2 mm by 2 mm. A microphoto of the chip is shown in Fig. 8.

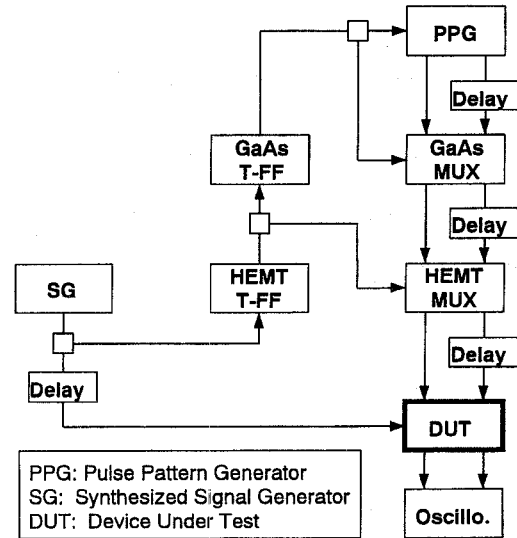


Fig. 9. Measurement setup.

IV. EXPERIMENTAL RESULTS

A. Measurement Setup

The fabricated chips were first measured on a wafer with dedicated 40-GHz bandwidth multiple contact probe heads. The measurement setup is schematically shown in Fig. 9. A complementary pair of the fundamental pseudo-random data streams (PN $2^{23}-1$) up to 10 Gbit/s were generated from a pulse pattern generator (PPG). These were quadrupled by using a GaAs MESFET 2:1 MUX unit and a HEMT 2:1 MUX module [2]. The complementary final bit-rate signals were input to the IC under measurement, with an appropriate delay for each other.

A master clock signal (up to 40 GHz) for the IC under test was generated by a synthesized signal generator. All the other clock signals (the half-rate clock for the HEMT MUX module and the quarter-rate clocks for the PPG and the GaAs MUX unit) were generated from the master clock using HEMT and GaAs MESFET T-FFs. This clock distribution scheme with a single clock source is the key to performing stable, low-jitter measurements at high bit rates. The complementary outputs of the MUX IC were monitored by a 50-GHz bandwidth digitizing scope, HP 54123-T, by way of 50-cm long, 40-GHz bandwidth coaxial cables.

B. Results and Discussion

First we performed the go/nogo test for all the chips by measuring the output eye opening at 60 Gbit/s. The yield was 48 % for the best wafer. A typical measured

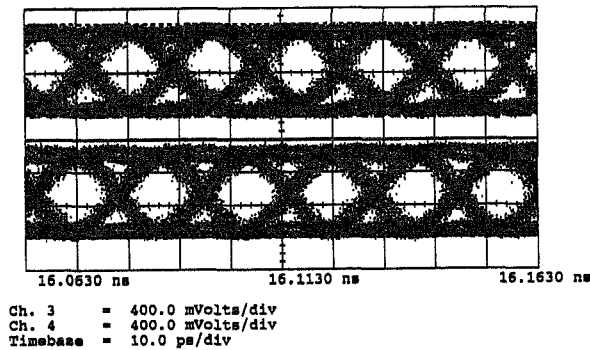


Fig. 10. Output eye diagrams at 60 Gbit/s.
 Upper: OUT; lower: /OUT.

eye pattern of the MUX IC output at 60 Gbit/s is shown in Fig. 10. Very clear eye opening is obtained. The voltage swing is 1100 mVp-p, which is sufficient for an SCFL interface. Error-free operation of the MUX IC will be confirmed in a subsequent measurement.

We attempted to measure the maximum operating speed for some chips. Figure 11 shows typical measured eye patterns of a MUX IC at 80 Gbit/s. Although insufficient bandwidth of the measurement instruments degrades the transition speed on the waveform, its eye opening is still clear. Error-free operation is expected at this bit rate. Much higher-speed operation near 100 Gbit/s is also expected.

The obtained circuit speed improvement over the previous report on 64 Gbit/s [6] owes much to the newly introduced high-speed, impedance-matched interconnection technology.

V. CONCLUSION

We report on an 80-Gbit/s 2:1 selector-type multiplexer IC using InAlAs/InGaAs/InP HEMTs incorporating a high-speed double-layer interconnection process with a low-permittivity insulator. The record operating data rate was measured on a 3-inch wafer. In spite of the bandwidth limitation on the measurement setup, clear eye patterns were successfully observed for the first time. Error free operation is well expected. The obtained circuit speed improvement over the previous record of 64 Gbit/s owes much to the newly introduced high-speed, impedance-matched interconnection technology. The dream of 100-Gbit/s electronic ICs is sure to be realized in the near future.

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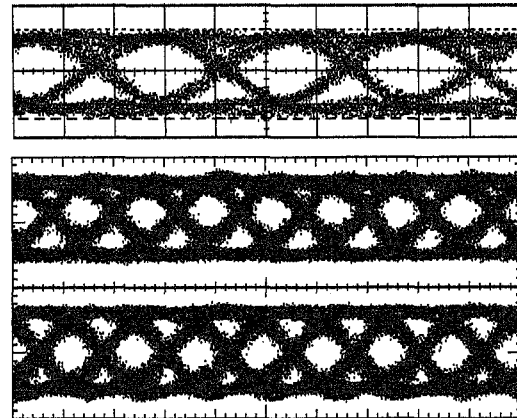


Fig. 11. Output eye diagrams at 80 Gbit/s. Upper: Input data;
 middle: OUT; lower: /OUT.

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